HITACHI

SERVICE MANUAL

TK No.2180E

# VT-89A

*Technical Information*

VHS

THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY VHS TYPE CASSETTES MUST BE USED.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

## VIDEO CASSETTE RECORDER

**October 1984** **TOKAI WORKS**

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## COMPARISON WITH CONVENTIONAL MODEL

| Item | VT-88A | VT-89A |
|---|---|---|
| Heads on cylinder<br>(Helical scan heads) | 5-head<br>Normal video: 2<br>FM-Audio: 2<br>Trick video: 1 | 7-head<br>SP Normal video: 2<br>LP/EP Normal video: 2<br>FM Audio: 2<br>Trick video: 1 |
| Fixed Audio Head<br>& Record/Play Processing | L/R independent<br>Record: Monaural<br>Play: Stereo | Same as on left |
| Cassette Loading | Front loading with<br>"Cassette In" indicator | Same as on left |
| Tape Remaining | 6-dash indication | Remaining time indication by OSD |
| Motors | 4 motors:<br>Single phase DD cylinder motor<br>DC capstan motor<br>DC loading motor<br>DC cassette loading motor | 5 motors:<br>3-phase brushless DD Cylinder motor<br>3-phase brushless DD Capstan motor<br>3-phase brushless DD Reel motor<br>DC Loading motor<br>DC Cassette loading motor |
| Recording Tape Speeds | 3 speeds (SP/LP/EP) | Same as on left |
| Still<br>Slow play<br><br>Frame advance<br>Double speed play<br>Visual Search<br><br>Reverse play | Field still<br>Impossible<br><br>Possible with remote control<br>Possible with remote control<br>Field search SP (x 3), EP (x 10)<br><br>Impossible | Same as on left<br>Variable slow play with slow tracking control<br>Same as on left<br>Field play<br>Frame search SP (x 5), LP (x 9), EP (x 15)<br>Possible |
| Program index | Impossible | Possible |
| Timer Recording | 6 programs/2 weeks | 8 programs/1 year (by 100-year-Calender timer $\mu$P) |
| Remote control (Number of buttons) | 13-mode wireless<br>(8 buttons) | 35-mode wireless<br>(32 buttons) |
| Timer Backup | 3 seconds | 60 minutes |
| Heater | Provided | Provided |
| Dew Sensor | Provided | Provided |
| Pause 5 Minutes Timer | Provided | Provided |
| IRT (Instant Recording Timer) | Provided | Provided |
| CATV | Provided | Provided |

| Item | VT-88A | VT-89A |
|---|---|---|
| Picture Control | Not provided | Provided (during playback) |
| OSD Function | Not provided | • Clock Setting<br>• Timer Record programming<br>• Tape Counter/Remaining time<br>• Clock, Date<br>• Operation mode<br>• Channel · AFT · Band |
| Noise Reduction for FM audio | PNR | Same as on left |
| Input Selection | Tuner/Simulcast/Aux. | Same as on left |
| Record Level Control | L/R independent slide control | Same as on left |
| ALC | With ON/OFF switch | Same as on left |
| Output Level Control | Rotary control | |
| Hi-Fi Indicator | Provided | Same as on left |
| Level Indicator | 2-sec peak hold digital indicator | Same as on left |
| Normal/Auto Audio Selector | Provided | Auto/Mix/Linear |

## 7-HEAD CYLINDER SYSTEM

### Outline

The 7-head cylinder has 5 video recording/playback heads and 2 audio recording/playback heads.

Fig. 1 shows the head composition.

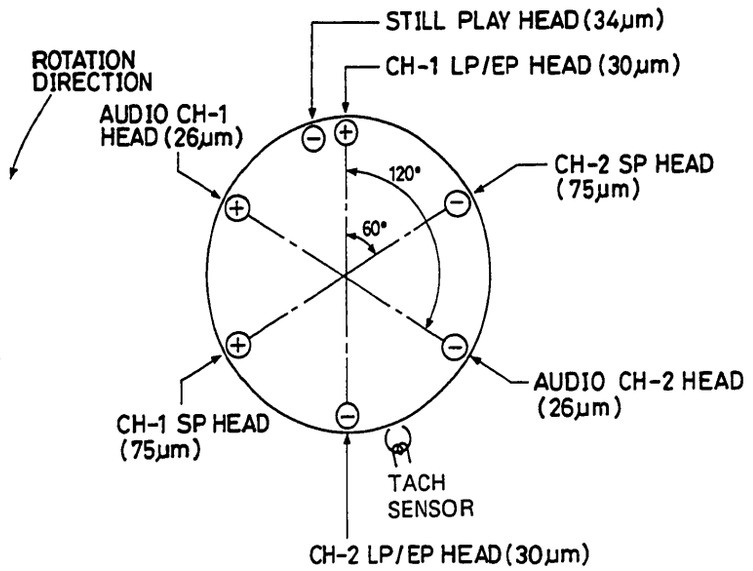
- CH-1 LP/EP and CH-2 LP/EP heads composing 1 pair of 2 heads (width: 30 μm) with different azimuth are provided for LP/EP video recording/playback.
- A trick play head (width: 34 μm) with the same azimuth as the CH-2 LP/EP head is provided in the position 2H away from the CH-1 LP/EP head so that field still play can be done when it is used together with the CH-2 LP/EP head.
- CH-1 SP and CH-2 SP heads (width: 75 μm) mechanically 120° advanced in phase from the LP/EP heads are provided for SP video recording/playback.
- Audio recording/playback heads (effective width: 26 μm) are provided mechanically 60° advanced in phase from the LP/EP heads.

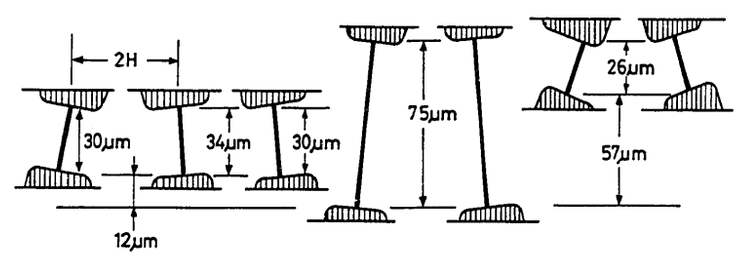
Fig. 2 shows the relation between the video track and audio track traced by the 7-head cylinder for different tape speeds. In the SP mode, the CH-2 video head traces the track the CH-1 audio head traces. Taking into consideration the fact that the track pitch is 58 μm, the audio track with the width of 26 μm is positioned approximately at the center of the video track width. To maintain this relation, the video CH-2 SP head is installed 120° delayed in phase with respect to the CH-1 audio head and with its level 57 μm lower.

In the EP mode, the CH-1 video head traces the track the CH-1 audio head traces, and in addition, it overlaps over the track next to the adjacent track. Taking into consideration the fact that the track pitch is only 19 μm, the CH-1 video head is installed 300° delayed in phase with respect to the CH-1 audio head and with its level 45 μm lower.

In the LP mode, it is depth-multiplex recorded by the LP/EP heads, so the track overlaps over the adjacent track. The relation of the level difference between the heads to the installation angle is determined when taking into consideration — recording over the different channels in the SP mode and depth-multiplex recording on the same channel in the EP mode.






| MODE \ HEAD | CH-1 LP/EP | STILL PLAY | CH-2 LP/EP | CH-1 SP | CH-2 SP | AUDIO CH-1 | AUDIO CH-2 |
|---|---|---|---|---|---|---|---|
| • Record/Play<br>• Search<br>• Rev. play | LP<br>EP | – | LP<br>EP | SP | SP | SP/LP/EP | SP/LP/EP |
| • Part of tape feed period in slow, F. advance modes | SP<br>LP<br>EP | – | SP<br>LP<br>EP | – | – | | |
| • Still<br>• Stop period in slow, F. advance modes<br>• Double speed play | – | SP<br>LP<br>EP | SP<br>LP<br>EP | – | – | | |

**Fig. 1 Cylinder Head Composition**

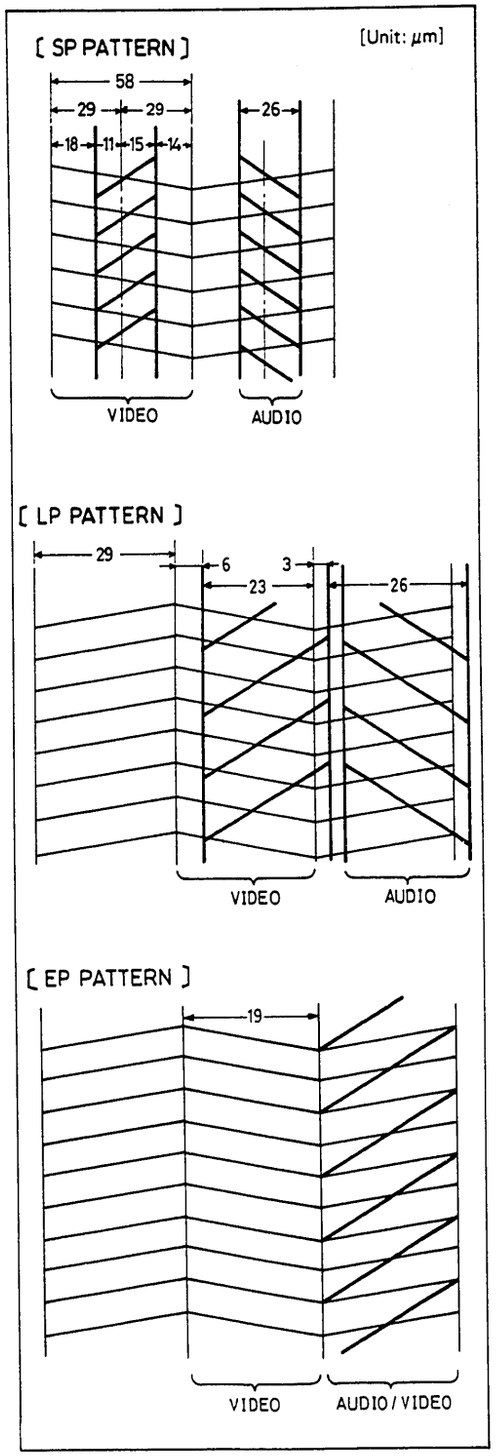



Fig. 2 Relationship between Video Track and Audio Track

**In the SP mode:**

- When the CH-2 SP head traces 120° after the CH-1 audio head, the difference of the track pitch is 58 μm x $\frac{120°}{180°} \fallingdotseq 39$ μm. When the CH-2 SP head is installed 39 μm lower than the CH-1 audio head, the left ends of both tracks are aligned.
- To position the left end of the video track at approx. 18 μm to the left of the audio track as shown in the figure, the CH-2 SP head should be installed 18 μm lower than the CH-1 audio head.
- As described above, when the CH-2 SP head is installed 39 μm + 18 μm = 57 μm lower than the CH-1 audio head, the track patterns shown in the figure are obtained.

**In the EP mode:**

- When the CH-1 LP/EP head traces 60° after the audio CH-1 head, the difference of the track pitch is 19 μm x $\frac{60°}{180°} \fallingdotseq 6$ μm. When the CH-2 SP head is installed 6 μm lower than the CH-1 audio head, the left ends of both tracks are aligned
- As for the video heads, since the SP heads and the LP/EP heads are installed with the level difference of approx. 12 μm so that their centers match during tracing in the NTSC standard, it is necessary to provide the 2-track (19 μm x 2 = 38 μm) component level difference in addition to the above for the audio and LP/EP video tracks of the same channel to overlap.
- As described above, a level difference of 38 μm + 6 μm = 44 μm is required.
  (The above numeric values are obtained by rounding first decimal place, so it differs a little from the level difference of 45 μm in the figure.)

## Recording Pattern

In VHS Hi-Fi recording, the video signal is surface re-recorded over the previously deep recorded audio signal. To do this depth-multiplex recording, a cylinder with 3 pairs of heads differing in phase by 120° is used.

Fig. 3 shows the process of forming the SP recorded pattern. In SP recording, the tape pattern resulting from the CH-2 audio head and the pattern from the CH-1 SP head overlap as shown in E). This pattern occurs as follows.

A) . . . The pattern tracked by the CH-2 audio head is a 26 μm width pattern with a guardband of 32 μm and azimuth of −30°.

B) . . . The pattern tracked by the CH-1 SP head becomes a 58 μm width pattern without a guardband and azimuth of +6°. When the CH-2 audio head starts tracing and passes two-third a field, the CH-1 SP head reaches the tracing start point of the CH-2 audio head.

E) . . . The level difference between the CH2 audio head and CH1 SP head is 68 μm, so when the CH-2 audio head moves by two-third a field after the cylinder starts, the center of the CH-2 audio head approximately matches the center of the CH-1 SP head. That is, the CH1 SP head tracks over the pattern recorded by the CH-2 audio head.

The same applies to recording by the CH-1 audio head and CH-2 SP head. The difference concerns azimuth; it is +30° with the CH-1 audio head, and −6° with the CH-2 SP head, so the pattern shown in E) is caused by the process shown in C) and D).

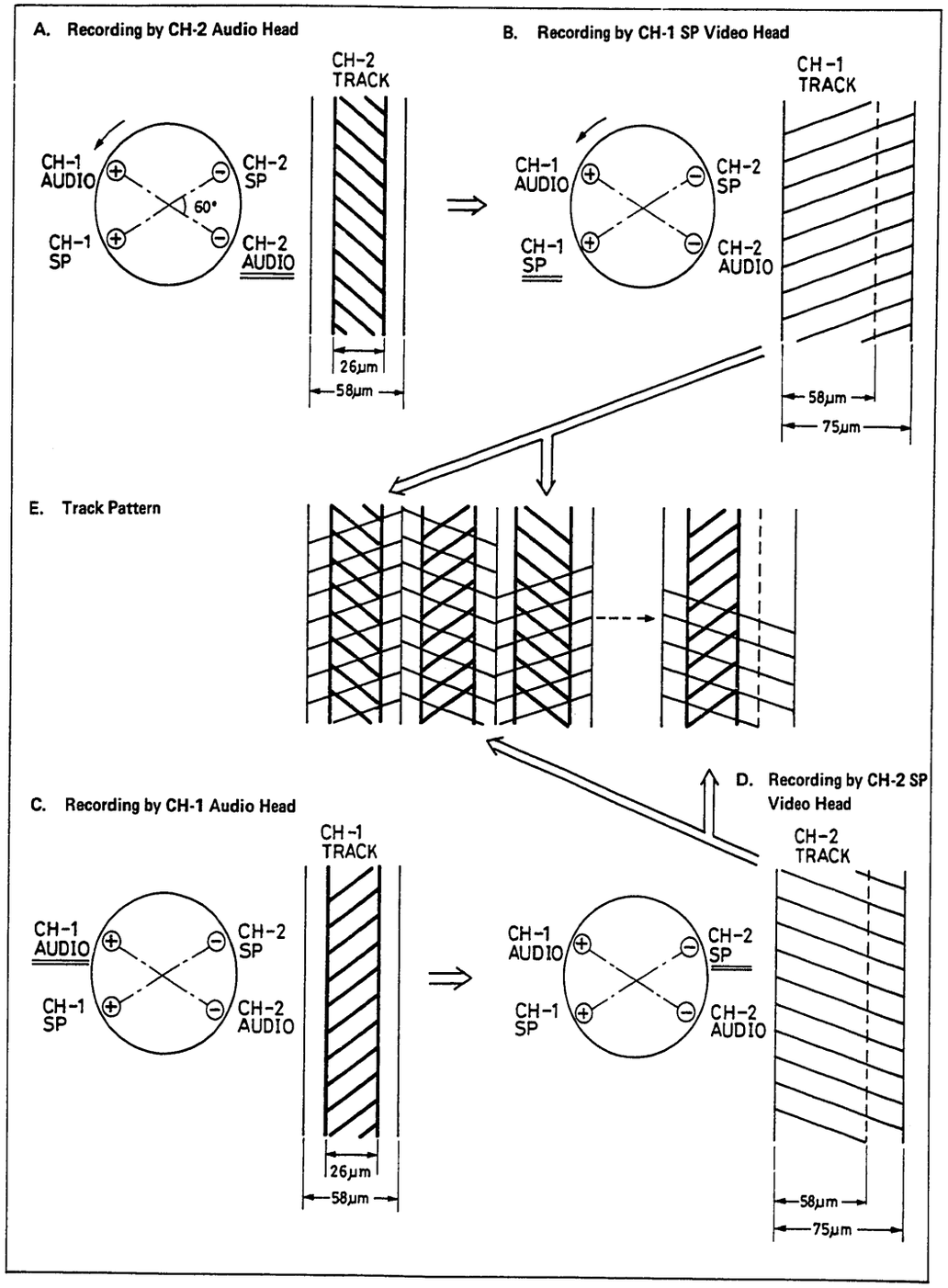



Fig. 3 Recording Pattern (SP mode)

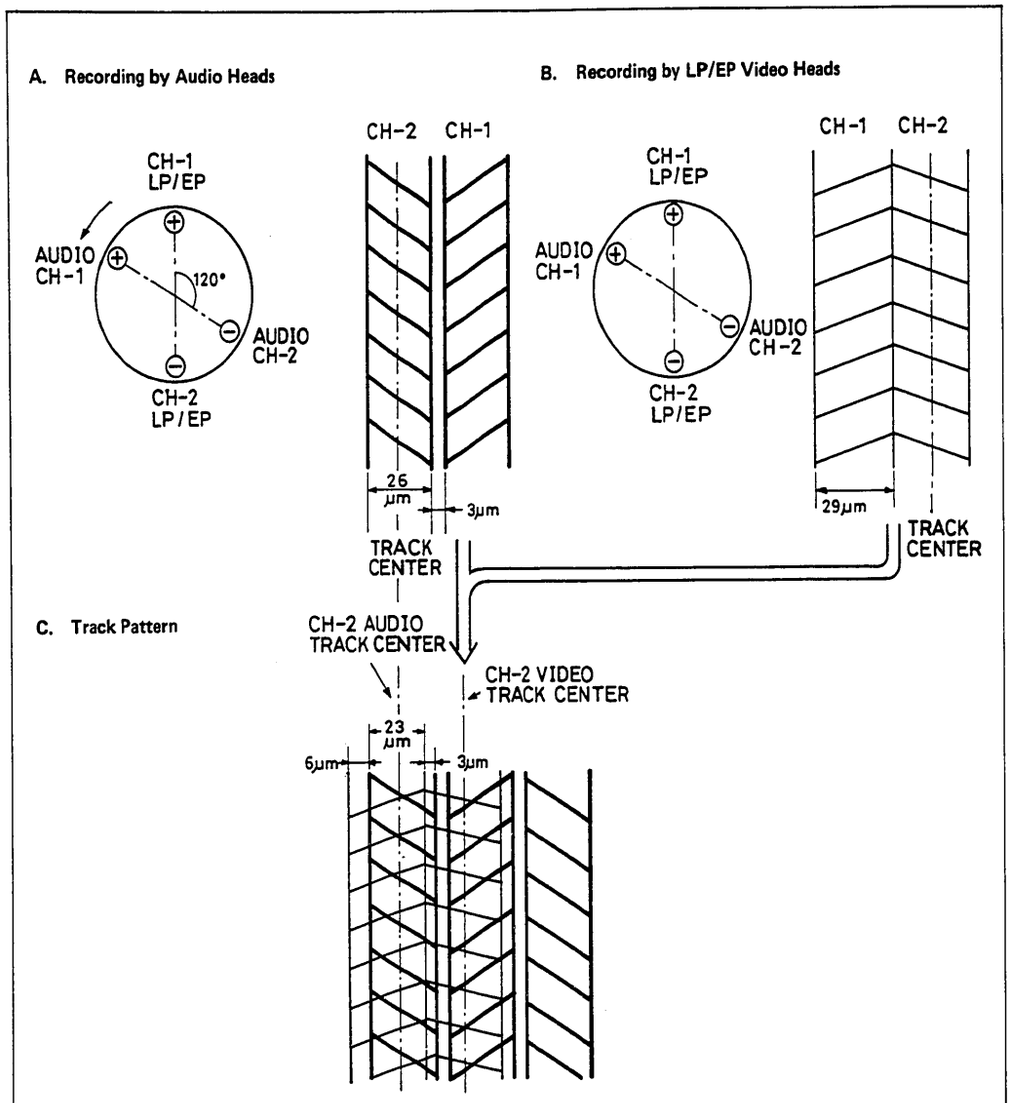



Fig. 4 Recording Pattern (LP mode)

Fig. 4 shows the process of forming the LP recorded pattern. The difference between the LP recording and the SP recording is that the tape feed speed in LP recording is half that in SP recording, so the pitch of the formed track is 29 μm. Taking this into consideration, in LP recording, the CH-2 LP/EP head installed with its phase 240° delayed compared to the CH-1 audio head overlaps the video signal over the pattern tracked by the CH-2 audio head and CH-1 audio head.

A) . . . The pattern tracked by the audio head is 26 μm with a guardband of 3 μm.

B) . . . The pattern tracked by the video head is 29 μm obtained by overlapping by 1 μm.

C) . . . In the LP mode, when the CH-2 audio head reaches the one-third point of tracing, the CH-2 LP/EP video head is positioned at approx. 6 μm from the left edge of the adjacent CH-1 audio track because the level difference between the 2 heads is 45 μm.



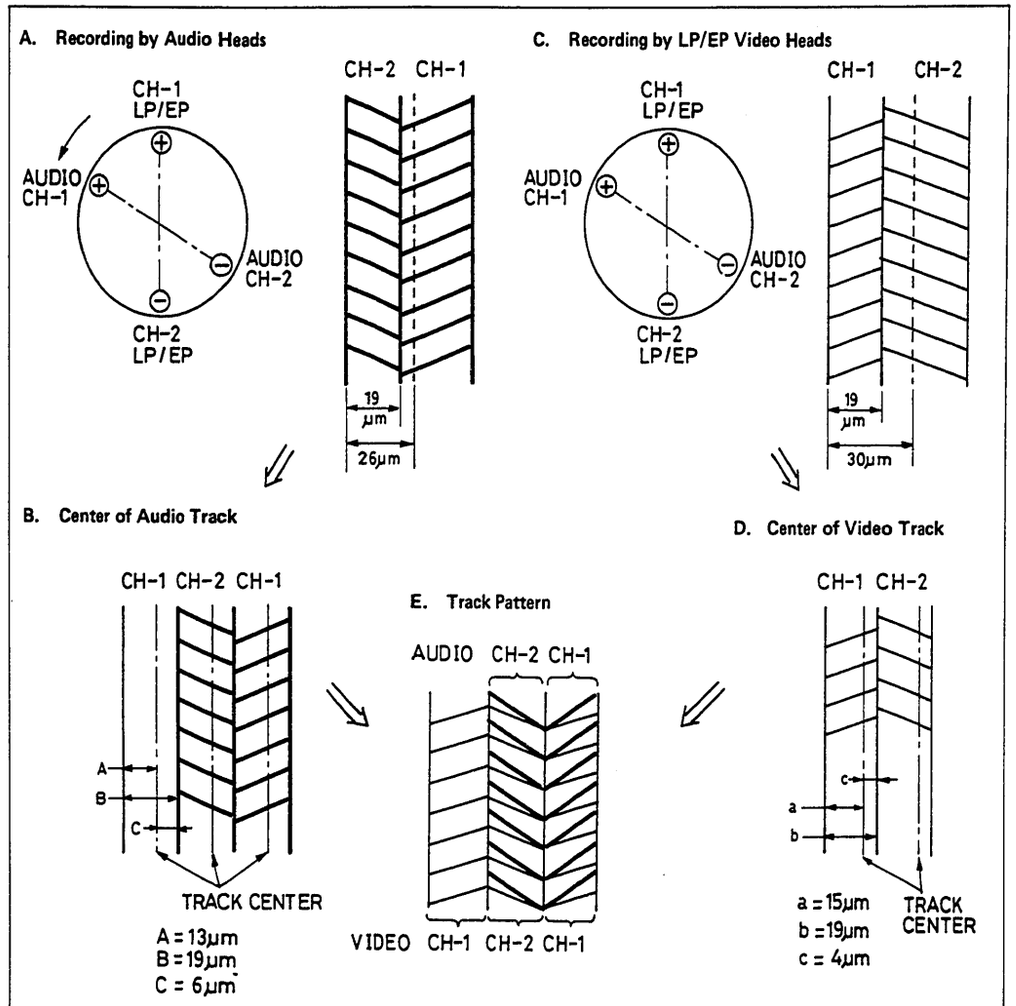



Fig. 5 Recording Pattern (EP mode)

Fig. 5 shows the process of forming the EP recorded pattern. The difference between EP recording and SP recording is that the tape feed speed in EP recording is 1/3 of that in SP recording, so the pitch of the formed track is 19 μm. Taking this into consideration, in EP recording, the CH-1 LP/EP video head installed with its phase 60° delayed compared to the CH-1 audio head overlaps the video signal over the pattern tracked by the CH-1 audio head. This track is the same channel track but it is 1H delayed. This causes the azimuth direction of the pattern to be negative.

A) . . . The pitch of the pattern tracked by the audio head is 19 μm and is formed with a 7 μm overlap.

B) . . . The pattern formed by the result of the above has the original center of the track positioned 13 μm from the left edge.

C) . . . Meanwhile, the pitch of the pattern tracked by the video head becomes 19 μm; it is formed with a 11 μm overlap.

D) . . . The pattern formed by the result of the above has the original center of the track positioned 15 μm from the left edge.

E) . . . The CH-1 LP/EP head has the level difference of 45 μm with respect to the CH-1 audio head and this is equivalent to 1 revolution of head +60° turn = 19 μm x 2 + 19 μm x 1/3 = 44 μm. The pattern is surface recorded by the CH-1 video head over the pattern deep recorded by the CH-1 audio head. The same applies to CH-2; in this case, the CH-2 video head overlaps the video signal over the pattern tracked by the CH-2 audio head.

## Composition of Video Heads

The video head cylinder of the VT-89 has 2 pairs of heads for the SP recording/playback and EP recording/playback and a head for field trick play (still, slow and double speed play).
Fig. 1 shows the construction of heads.
Visual search and reverse play as well as normal recording/playback are done by the pair of SP heads, and the still, slow and double speed plays are for field trick play using the still head and CH-2 LP/EP head.

### Head Switching

Fig. 6 shows the head switching circuit.
The switching circuit is composed of an relay circuit (RL201) and IC204 installed in the Y/chroma circuit, and is operated by the signals obtained from the servo circuit.

### Operation of relay (RL201)

RL201 switches the 2 pairs of heads between the SP and EP (LP) modes. The relay is driven by Q208 and the switching signal is supplied from the servo circuit.
The signal obtained at IC606 pin 11 becomes Hi in the double speed play, slow, still and frame advance modes. Q209 is gated by this signal to drive Q208. Q208 is activated in the record, play, search and reverse play modes and switches the relay to the SP side.
This relay operates as follows.

| Q208 | RL201 | Active Heads | Operation Mode |
|---|---|---|---|
| ON | SP side | CH-1/CH-2 SP heads | SP recording, play, search, reverse play |
| OFF | $\overline{SP}$ side | CH-1/CH-2 LP/EP heads | LP/EP recording, play, search, reverse play |
| | | CH-2 LP/EP head | SP/LP/EP double speed play, slow, still |

### Operation of IC204

IC204 performs switching between recording and play, and switching of the still head. Switching between recording and play is done by Q5 and Q6 and switching of the CH-1 head and still head is done by Q1, Q3 and Q4. IC204 performs switching between recording and play using the REC 9V signal supplied to pin 11, and switching of the still head using the "HEAD SWITCH" signal obtained from the servo circuit and the double speed play mode signal "2X". The operation of IC204 is as follows.

| Mode | Switch turned ON | Remarks |
|---|---|---|
| Recording | CH-1 system: Q1/Q5/Q3<br>CH-2 system: Q6 | Still head switched off |
| • Play, search, reverse play<br>• Part of tape feed period in slow, frame advance modes | CH-1 system: Q1/Q3<br>CH-2 system: – | Still head switched off |
| • Still, double speed play<br>• Tape stop period in slow, frame advance modes | CH-1 system: Q4<br>CH-2 system: – | CH-1 heads switched off |

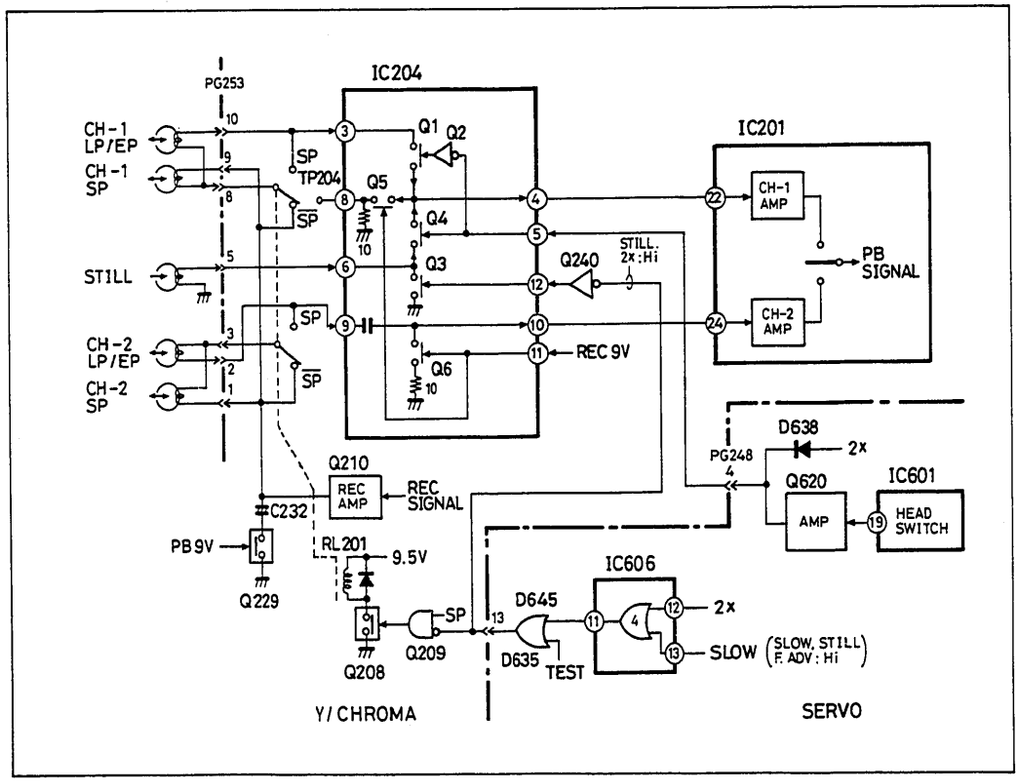



Fig. 6 Head Switching Circuit



## Signal Route in Each Mode

### Record mode

CH-1
REC SIGNAL: Q210 → <SP> → PG253-9 → CH-1 SP HEAD → PG253-8 → RELAY: SP → IC204-3 →
REC SIGNAL: Q210 → <EP> → RELAY: $\overline{SP}$ → PG253-8 → CH-1 LP/EP HEAD → PG253-10 → IC204-3 →
→ Q1 → Q5 → GND

CH-2
REC SIGNAL: Q210 → <SP> → PG253-1 → CH-2 SP HEAD → PG253-3 → RELAY: SP →
REC SIGNAL: Q210 → <EP> → RELAY: $\overline{SP}$ → PG253-3 → CH-2 LP/EP HEAD → PG253-2 →
→ IC204-9 → Q6 → GND

### Play, visual search, reverse play modes

Q229 is activated in the play mode to form the play route.

CH-1 SP PLAY SIGNAL: CH-1 SP HEAD → PG253-8 → RELAY: SP →
CH-1 LP/EP PLAY SIGNAL: CH-1 LP/EP HEAD → PG253-10 →
→ IC204-3 → Q1 → IC204-4 →
→ IC201-22

CH-2 SP PLAY SIGNAL: CH-2 SP HEAD → PG253-3 → RELAY: SP →
CH-2 LP/EP PLAY SIGNAL: CH-2 LP/EP HEAD → PG253-2 →
→ IC204-9 → IC204-10 → IC201-24

### Double speed play, still, slow, frame advance modes

The play route is formed by activation of Q229 as the basic mode is play.

CH-1 SIDE PLAY SIGNAL:

(During tape stop period in double speed play, still, slow, frame advance modes)

STILL HEAD → PG253-5 → IC204-6 → Q4 →

(During the tape feed period in slow/frame advance modes)

CH-1 LP/EP HEAD → PG253-10 → IC204-3 → Q1 → IC204-4 → IC201-22

CH-2 SIDE PLAY SIGNAL:

CH-2 LP/EP HEAD → PG253-2 → IC204-9 → IC204-10 → IC201-24

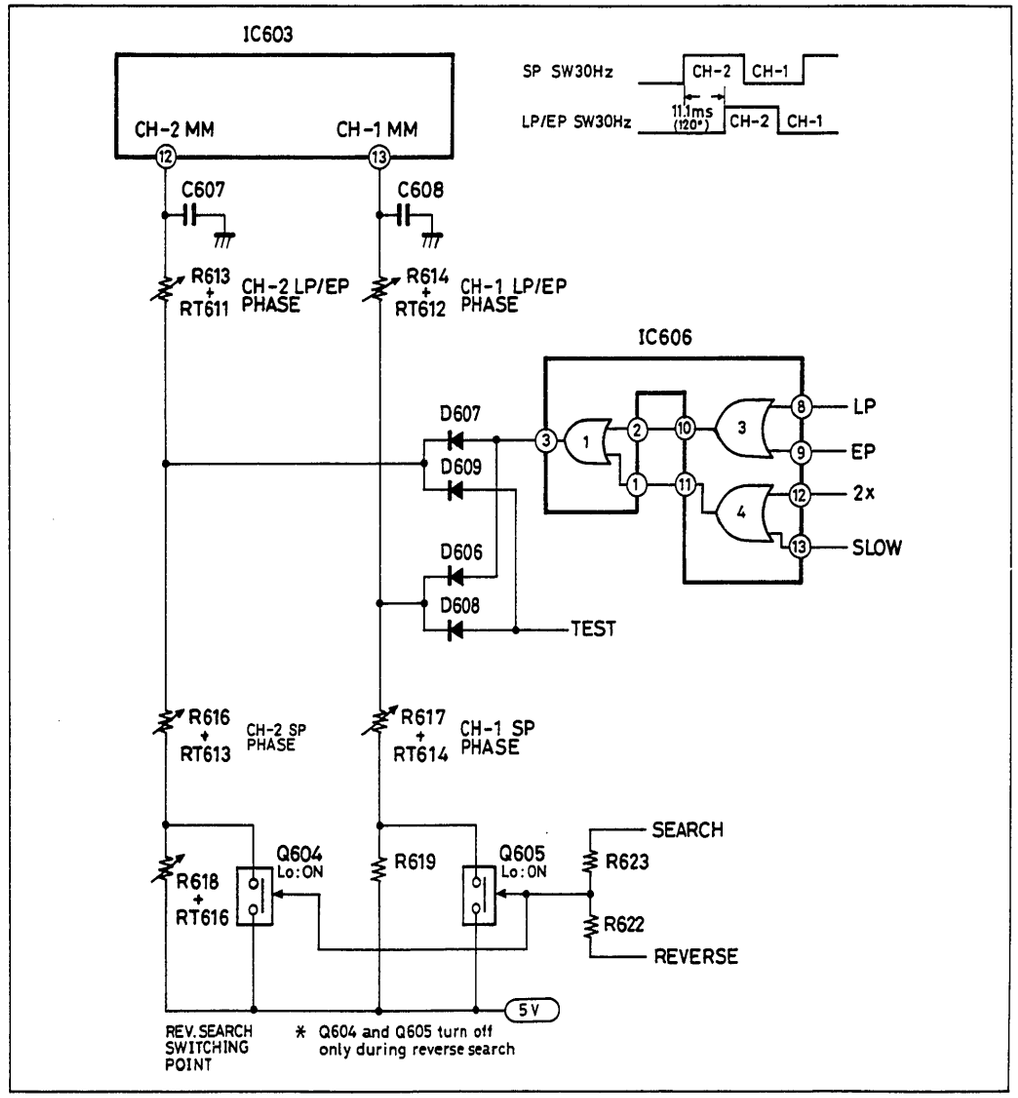



**Fig. 7 SW30Hz Generation Circuit**

## Video Head Switching Point

In the 7-head cylinder, the LP/EP heads are installed mechanically 120° delayed with respect to the SP heads. The SW30Hz generator (in IC603) in the servo circuit obtains the SP SW30Hz pulse from the detection point of the tach pulse, and the LP/EP head switching point is set to the point 120° delayed further from this point.

Fig. 7 shows the SW30Hz generator circuit.

IC603 determines the rise (CH-2 switching point) of the SW30Hz pulse from pin 12, and determines the fall (CH-1 switching point) of the SW30Hz pulse from pin 13.

IC606, D607 and D606 compose the switching point circuit for the recording, play, search and reverse play in the LP/EP modes and the field play (slow, still, double speed play) in the SP/LP/EP modes, and RT611 determines the switching point of the CH-2 LP/EP head and RT612 determines that of the CH-1 LP/EP head.

Q604 and Q605 compose the switching point circuit for the recording, play, forward search and reverse play in the SP mode in which they are turned on, and RT613 determines the switching point of the CH-2 SP head and RT614 determines that of the CH-1 SP head.

Q604 and Q605 turns off in the SP reverse search mode, and RT611 determines the switching point of the CH-2 SP head and R619 (solid resistor) determines that of the CH-1 SP head.

## FM Audio Head Switching Pulse Generation

The FM audio heads are related to the video heads as shown below.

60° delayed with respect to the SP video heads.

60° advanced (300° delayed) with respect to the LP/EP video heads.

From the relationship shown above, the switching points of the FM audio heads can also be obtained by delaying and advancing the switching pulses for the video heads by the components shown above. The FM audio head switching pulse is obtained from the SW30Hz pulse in IC2003 on the FM audio board in this system.

Fig. 8 shows the FM audio head switching pulse generation circuit. This circuit is composed of the 2-stage monostable multivibrators. The fall of the CH-1 pulse in the SP mode is determined by RT2002 and the rise of the CH-2 pulse is determined by RT2001. In the LP/EP modes, when the rise of the CH-2 pulse is determined by RT2001, the fall of the CH-1 pulse is automatically determined by the amount of variation of RT2002 set in the SP mode.

IC2003 incorporates 2 flip-flops; by providing a time constant circuit at pins 1 and 2, the pulse width of the initial stage circuit can be regulated and by providing a time constant circuit at pins 14 and 15, the pulse width in the latter stage circuit can be regulated. The respective inputs are; pins 4 and 5 for the initial stage and pins 11 and 12 for the latter stage. The truth table of this element is as shown in the figure.

As can be seen from this, it can be used as a monostable multivibrator by fixing pin A to Lo and applying a pulse to pin B, or fixing pin B to Lo and applying a pulse to pin A. The FM audio head switching pulse is obtained by delaying the SW30Hz pulse using the 2-stage monostable multivibrators.

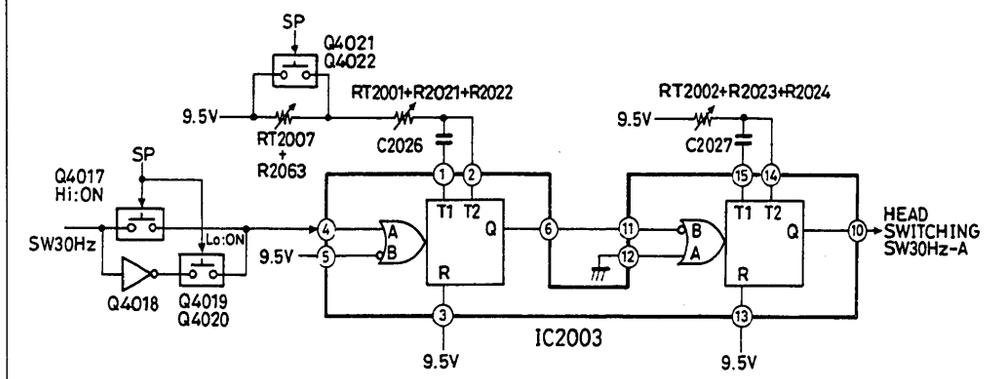
- The initial stage monostable multivibrator regulates the delay of the pulse, and
- The pulse width is regulated by the second monostable multivibrator.

The following can be obtained for different modes as shown in the timing chart.

In the SP mode, the SW30Hz pulse applied to pin 4 has positive phase because Q4017 turns on, and the operation amount of the monostable multivibrator is determined by RT2001 because switches Q4021/Q4022 turn on. That is, the pulse with the delay amount (60 ° ) determined by RT2001 with respect to the SW30Hz pulse is obtained as SW30Hz-A.

In the LP/EP modes, the input SW30Hz pulse is previously inverted to obtain the phase difference of 300°, and the SW30Hz-A pulse is obtained by applying the 120° delay operation.

Since switches Q4019/Q4020 turn on in the LP/EP modes and Q4017 turns off, the input pulse is inverted by Q4018 and is given reverse phase. With this operation, 180° delay is provided. Further, switches Q4021/Q4022 turn off, RT2007 becomes effective, and the delay (determined by RT2001) in the SP mode is given a further 60° delay.




Unit Monostable Multivibrator Truth Table

| A | B | Q | $\bar{Q}$ |
|---|---|---|---|
| ↑ | Hi | ⊓ | ⊔ |
| ↑ | Lo | Q | $\bar{Q}$ |
| Hi | ↓ | Q | $\bar{Q}$ |
| Lo | ↓ | ⊔ | ⊓ |

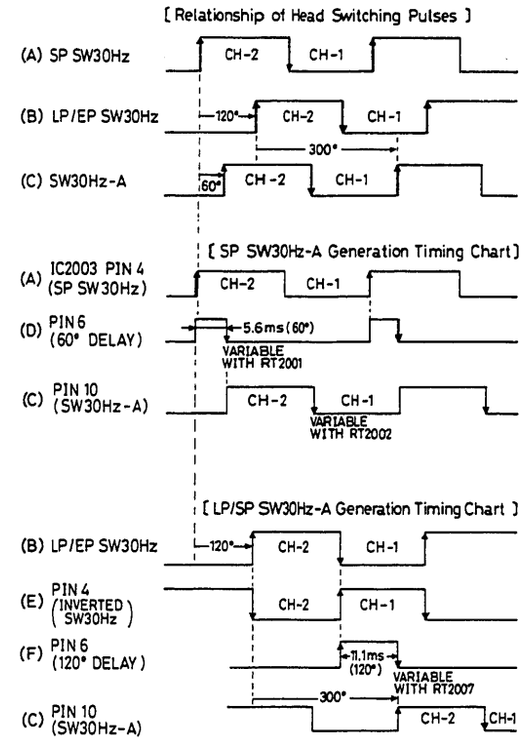



**Fig. 8 FM Audio Head Switching Pulse Generation Circuit**

## Audio Circuit Recording/Playback Operation

The recording/playback routes of the audio signal are the monaural recording/stereo playback system using the fixed heads and the stereo FM recording/playback system using the rotary heads.

| Audio Track | Recording | Playback |
|---|---|---|
| LINEAR TRACK | MONAURAL (Monaural recording with stereo input) | STEREO (Tapes recorded on this unit is played back in monaural) |
| Hi-Fi TRACK | STEREO | STEREO |

The following monitor sounds are obtained in each mode.

| Mode | AUTO/MIX/LIN Switch | Tape, Condition, etc. | Monitor Output |
|---|---|---|---|
| PLAY | AUTO | FM recorded tape | Hi-Fi (Hi-Fi indication) |
| | | Non FM recorded tape | Linear |
| | MIX | FM recorded tape | Hi-Fi + Linear (Hi-Fi indication) |
| | LINEAR | Not concerned | Linear |
| A. DUB | Any position | – | Hi-Fi + Linear EE audio (Hi-Fi not indicated) |
| A. DUB PAUSE | Any position | – | Linear EE audio |
| REC STOP | Any position | Microphone used | Hi-Fi + Linear EE audio (Hi-Fi not indicated) |
| | Any position | Microphone not used | Hi-Fi EE audio |

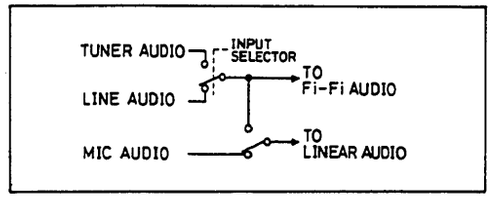
### Recording Audio Input

The audio recording condition in each recording mode is as follows.

| | |
|---|---|
| RECORD | LINEAR<br>Hi-Fi |
| A. DUB | LINEAR<br>* Prerecorded Hi-Fi audio is not erased. |
| V. DUB | * Prerecorded linear audio is not erased.<br>* Hi-Fi audio is erased. |

The input audio signals are:
- Tuner audio
- Line audio
- Microphone audio

The relation between them is as follows.




As can be seen, the tuner audio and line audio are supplied to the Hi-Fi audio system, and the tuner audio, line audio and microphone audio are supplied to the linear (normal) audio system.
The microphone audio signal is used for audio dubbing. Audio dubbing is the operation to record audio signal on the linear track, and the audio recorded on the Hi-Fi track is not erased but is left as it was previously recorded. The tuner audio and line audio are selected by the input select circuit (IC502) and are controlled by the selector switch (AUX/SIMUL/TUNER: S852). The input relation for all switch positions are as follows.

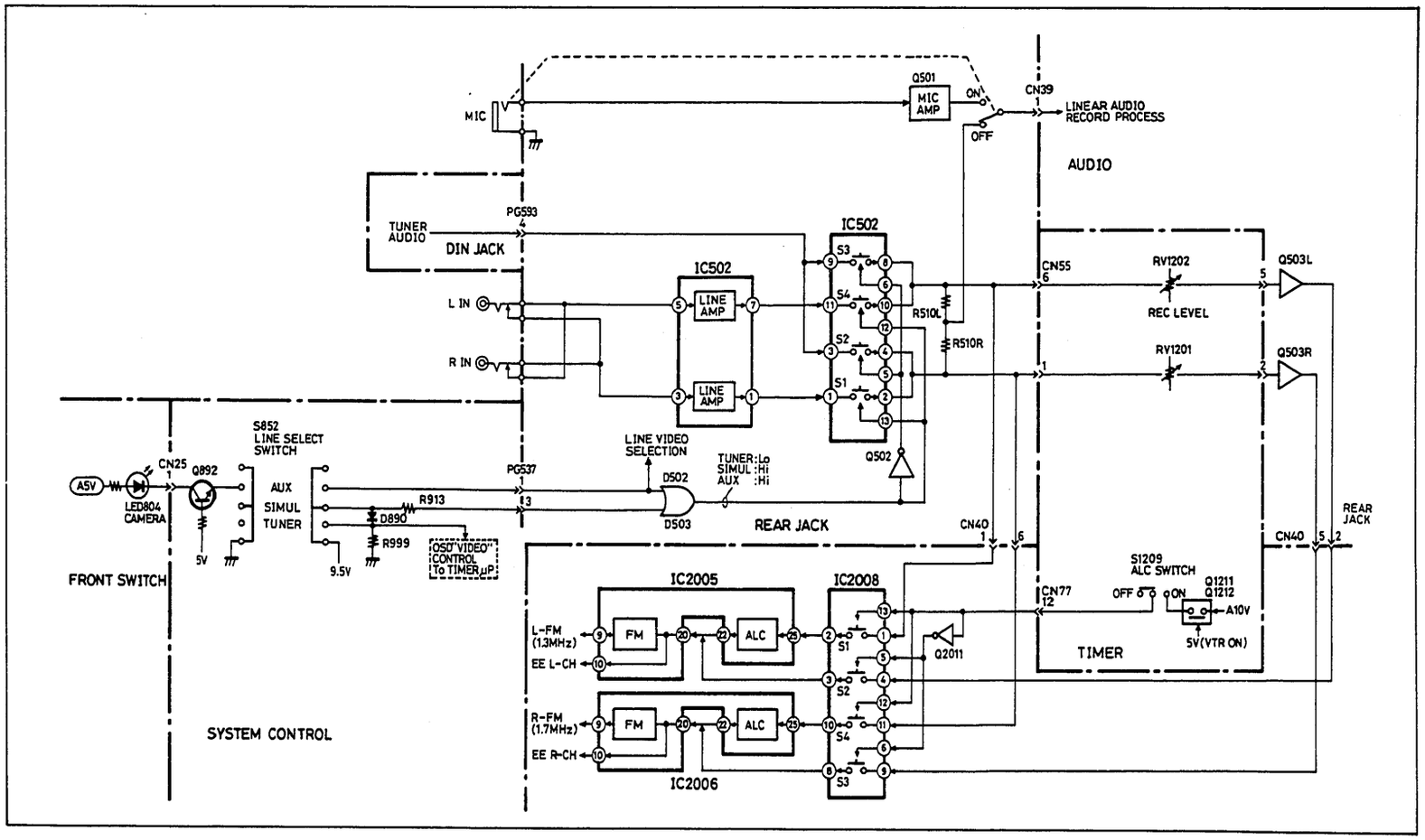



Fig. 1 Recording Audio Input Circuit

| S852 position | Active switch in IC502 | Output Signal of IC502 | Video signal | Display |
|---|---|---|---|---|
| TUNER | S2, S3 | Tuner audio is supplied to:<br>•the Hi-Fi system separately for L and R channels,<br>•the linear system with L + R mixed. | Tuner video | "VIDEO" is displayed on the monitor screen in the OSD mode. |
| SIMUL-CAST | S1, S4 | Line audio is supplied to:<br>•the Hi-Fi system separately for L and R channels,<br>•the linear system with L + R mixed. | •SIMUL position: Tuner video signal is selected. | • SIMUL position: "VIDEO" is displayed in the OSD mode. |
| AUXILIARY | | When only one jack is connected with external equipment, the connected input is sent to:<br>•the Hi-Fi system separately for L and R channels,<br>•the linear system the channel of which the equipment is connected. | • AUX position: Line video signal is selected. | • AUX position: "CAMERA" indicator lights. |

The output from IC502 is supplied to the linear system and Hi-Fi system as follows.

LINEAR system: The output from IC502 is mixed by R510L/R, and supplied to the linear system via the microphone jack. The microphone jack incorporates a switch and the microphone input has priority over the output from IC502.

Hi-Fi system: The output from IC502 is sent to the ALC and manual recording systems separately for the L and R channels, and then is supplied to the FM modulation circuit. The ALC or manual recording system is selected by IC2008 in the FM audio circuit. This selection is controlled by the ALC switch (S1209) on the timer circuit board. The signal routes of both systems are as follows.

MANUAL RECORDING

L-CH: IC502 PINS 8/10→CN55 PIN 6→RV1202: REC LEVEL→
R-CH: IC502 PINS 2/4→CN55 PIN 1→RV1201 →
REAR JACK BOARD→| |← TIMER BOARD→|

→CN55 PIN 5→Q503L→CN40 PIN 2→IC2008 PIN 4→
→CN55 PIN 2→Q503R→CN40 PIN 5→IC2008 PIN 9→
|← REAR JACK BOARD →| |← AUDIO BOARD

→S2→PIN 3→IC2005 PIN 20→L-CH REC PROCESS
→S3→PIN 8→IC2006 PIN 20→R-CH REC PROCESS
|← AUDIO BOARD →|

ALC RECORDING

L-CH: IC502 PINS 8/10→CN40 PIN 1→IC2008 PIN 1 → S1→
R-CH: IC502 PINS 2/4→CN40 PIN 6→IC2008 PIN 11→S4→

→PIN 2→IC2005 PIN 25→L-CH ALC REC PROCESS
→PIN 10→IC2006 PIN 25→R-CH ALC REC PROCESS

As for the signals supplied to the FM modulation system, the L-CH signal modulates the 1.3 MHz carrier and is output via IC2005 pin 9, and the R-CH signal modulates the 1.7 MHz carrier and is output via IC2006 pin 9, and they are sent to the next stage. At the same time, parts of the signals before being modulated are derived from pins 10 of respective ICs as EE audio signals and are sent to the output system.

ALC ON/OFF selection is performed by the ALC switch (S1209) on the timer board. The input to the switch is the "VTR ON" signal obtained at Q1211/Q1212. 5V is applied to Q1211/Q1212, and this is the power source generated when the power switch of the VTR is turned on, so the "VTR ON" signal is obtained at Q1211/Q1212. This signal is supplied via S1209 to the switch selection control pin of IC2008.

| ALC switch position | Active switches in IC2008 | Reason |
|---|---|---|
| ON | S1 for L-CH<br>S4 for R-CH | IC2008 pins<br>12 and 13: Hi |
| OFF | S2 for L-CH<br>S3 for R-CH | IC2008 pins<br>4 and 9: Hi |

**Playback Audio Output**

The sound to be played back is shown below according to the mode in which the recording was done when playing a tape recorded with the same recorder.

| Mode during recording | Played back sound |
|---|---|
| RECORD<br>A. DUB | LINEAR (MONAURAL)<br>Hi-Fi (STEREO) |
| V. DUB | LINEAR<br>* Hi-Fi is not recorded |

Fig. 2 shows the playback audio output circuit.
The audio signal is played back by 4 heads.

- 2 heads are the conventional fixed heads and are used for L and R channel tracks, and,
- The other 2 heads are the helical-scanning FM audio heads installed on the cylinder and are used for CH-1 FM audio/CH-2 FM audio.

The signals detected by the fixed heads are processed in the audio circuit separately for the L and R channels. The detected signals are amplified by the preamplifier IC402 L/R and are supplied to the output select circuit IC2010.
Playback of Hi-Fi audio uses the signals detected by the helical-scanning heads, and is performed in the FM audio circuit. Signals detected by the CH-1/CH-2 heads are amplified and combined by IC2001. The FM wave combined into a continuous signal via IC2001 is demodulated to an audio signal by IC2005/IC2006. The demodulated Hi-Fi audio signal is sent to the output select switch (IC2010).
Hi-Fi/linear selection of the playback audio signal thus applied to IC2010 is performed by S1/S4 (for linear audio) and S2/S3 (for Hi-Fi audio). S2 and S3 are changed over according to the level at pins 5 and 6, and S1 and S4 are changed according to the level at pins 12 and 13.

IC2010 outputs the Hi-Fi audio during FM playback (for example, when playing an FM recorded tape with the output select switch set to AUTO), and outputs the linear audio during linear playback (for example, when playing a prerecorded tape with the output select switch set to LINEAR).

IC2010 outputs the mixed audio of the Hi-Fi and linear tracks during mixed playback (for example, when playing an FM recorded tape with the output select switch set to MIX). The details are described later. The linear system and Hi-Fi system of the audio signal obtained in this way are formed into one system, and sent to the amplifiers in IC2007 separately for the L and R channels. One output from IC2007 is sent to the level display becoming the indication data for the display during recording and playback. The other output is sent to the headphone jack, line jack and the RF converter via the muting circuit composed of Q2013 L/R.

Headphone jack: Sound with its output level varied by the volume control can be monitored from the headphone jack. Sound from the L-CH alone can be monitored by inserting a plug into the earphone jack.

Line out jack: When both line out jacks are connected, L and R channels can be monitored separately, and when only one line out jack is connected, the sound output from the connected plug becomes (L + R).

RF converter: The mixed output from the line out amplifiers Q508 L/R is supplied to the RF converter.

**Selection between Hi-Fi audio and linear audio**

S1/S4 and S2/S3 in IC2010 are switched over according to the input levels at pins 5, 6, 12 and 13.

The signals fed to pins 12 and 13 are the "LINEAR" signals (signals used to select the linear audio signals) and the signals applied to pins 5 and 6 are the "FM" signals (signals used to select the Hi-Fi audio signals); both of them are obtained in a circuit in the system control circuit.
Fig. 3 shows the audio output control signal generation circuit. The "LINEAR" signal becomes Hi under the following conditions to select the linear audio.

The "FM" signal becomes Hi under the conditions in the table on page 19 to select Hi-Fi audio.

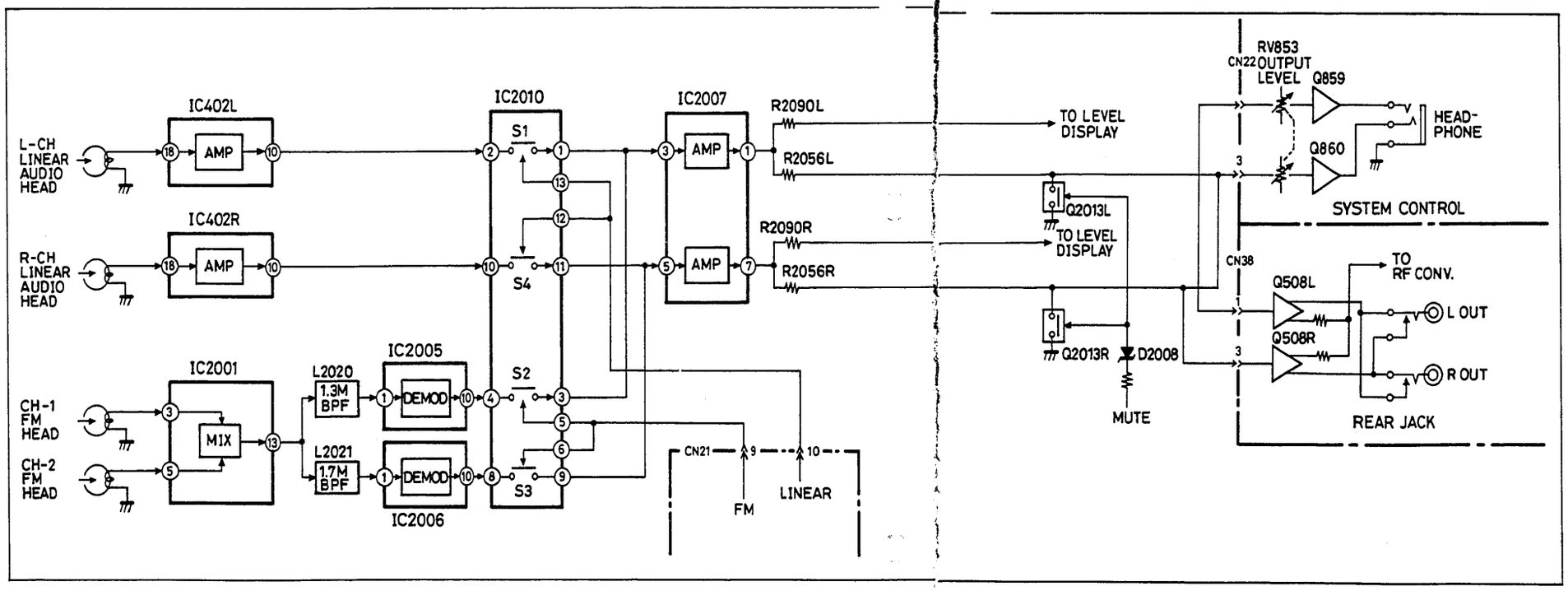



Fig. 2 Playback Audio Output Circuit

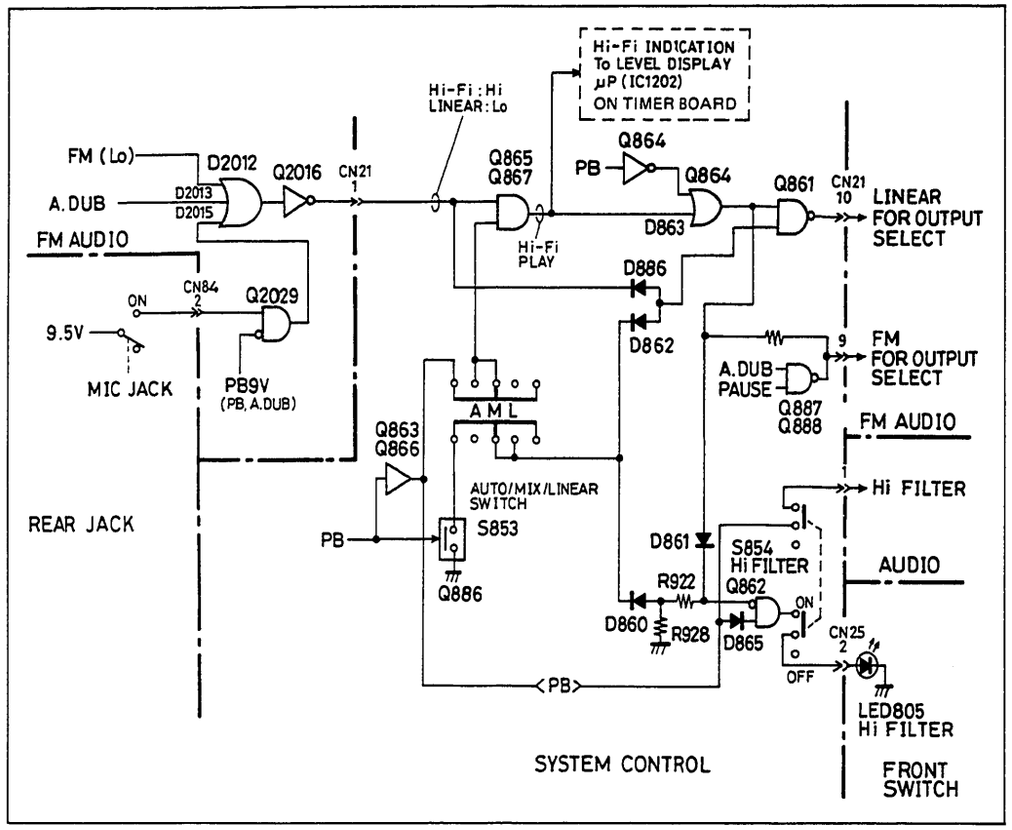



**Fig. 3 Audio Output Control Signal Generation Circuit**

| Condition | | | Signal generation route |
|---|---|---|---|
| Mode | S853 | Others | |
| PLAY | LINEAR or MIX | — | PB→Q886: ON, MIX/LINEAR→ → D862 CATHODE: Lo→ →Q861: Hi OUTPUT→CN21 PIN 10: Hi |
| PLAY | AUTO | Recorded tape without FM | FM(Lo): Hi→D2012→Q2016: Lo OUTPUT→ →D886 CATHODE: Lo→Q861: Hi OUTPUT |
| A. DUB (monitor) | Any position | — | A. DUB: Hi→Q2016: Lo OUTPUT→ →Q861: Hi OUTPUT |
| REC (monitor) | Any position | Microphone connected | REC, MIC connected→CN84 PIN 2: Hi → →Q2029: Hi→OUTPUT→D2015→ →Q2016: Lo OUTPUT→D886→Q861: Hi OUTPUT |



| Condition | | | Signal generation route |
|---|---|---|---|
| Mode | S853 | Others | |
| PLAY | AUTO or MIX | FM recorded tape | PB→Q2029: Lo OUTPUT→D2015 ANODE: Lo; FM recorded tape→FM: Lo→D2012 ANODE: Lo → →Q2016: Hi OUTPUT; S853: AUTO/MIX, P→Q863/Q866 → →Q865/Q867: Hi OUTPUT→ →D863→CN21 PIN 9: Hi |
| A. DUB, REC STOP | Any position | — | Q864: Hi OUTPUT→CN21 PIN 9: Hi |

The "FM" signal becomes Lo under the following condition to automatically stop the Hi-Fi audio output.

Audio dub pause mode

CN21 pin 9 is forcibly set to Lo by Q887 and Q888.

**"Hi-Fi" Indication Control**

"Hi-Fi" is indicated in the timer/level display while playing back Hi-Fi sound.

This shows that Hi-Fi sound is being played back when an FM recorded tape is played back with the output select switch (S853) set to AUTO or MIX, and "Hi-Fi" is indicated. As shown in the table above, when an FM recorded tape is played back and S853 is set to AUTO or MIX, Q865 and Q867 output Hi and is sent to the level display μP (IC-1202). This causes the μP to display "Hi-Fi".

**Hi Filter Switch Operation**

The Hi filter switch (S854) eliminates frequencies of more than 5 kHz in the linear audio and suppresses high-frequency noise during play. When the Hi filter is operating with linear audio output, the Hi Filter indicator (LED805) lights. The linear audio output without Hi-Fi audio is obtained when S853 is set to the LINEAR position or when S853 is set to MIX or AUTO and a tape without FM is played back.

When S853 is set to the LINEAR position in the play mode, Q862 is turned on by D860, and LED805 is lit via S854. When a tape without FM is played back, the anode of D861 becomes Lo, Q862 is turned on and LED805 is lit.

**Muting Operation**

The muting operation is done when Q2013 L/R turn on and this becomes effective in the following cases.

- Pop noise due to power switching
- Noise occurring at the coupling section when shifting modes.
- Muting during trick play
- When the program button on the remote control hand unit is operated so the OSD mode is entered.
- Dropout noise caused by lack of FM envelope.

Fig. 4 shows the muting signal generation circuit.

When the power is supplied (power switch ON), Q505 outputs Hi for a time determined by R547 x C514 just after the 9.5V rises by the muting circuit composed of ZD504/Q505 and the muting signal is generated.

At the coupling section between modes and during trick play, Q2014 is turned on by the output (Lo) at pin 24 of the system control μP (IC851) via ZD855, and the muting signal is generated.

When the OSD mode is entered by the program button operation, the sound is muted by the output from pin 2 of the character generator (IC52) in the system control circuit.

Muting is performed by the LINE MUTE signal* when tracking drifts too much.

* LINE MUTE signal: This is obtained from the FM audio circuit, and is set to Lo when the FM envelope drops too much from the specified level. This drop is approx. 10 dB - 15 dB from 1/3 to 1/5 approximately. When the FM drop is more than the above, it is judged that there is no FM envelope, the FM AUTO signal returns to Hi, and the playback output is obtained from the linear audio track.

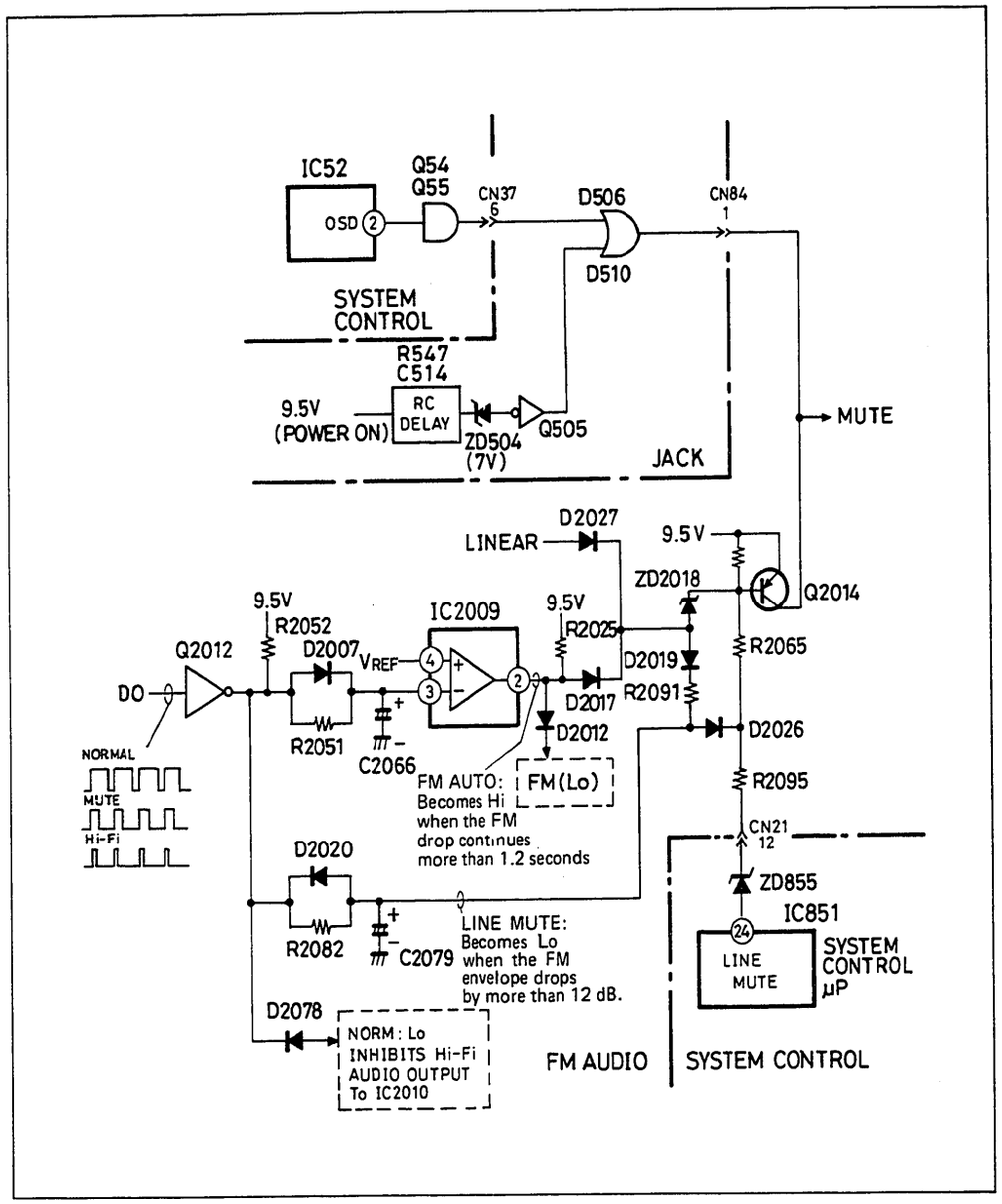



Fig. 4 Mute Signal Generation Circuit



**Muting caused by FM drop**

The DO pulse width is narrow and the "on" period of Q2012 is short during FM audio playback. The voltage C2066 during the "off" period of Q2012 is discharged via R2051 during the "on" period.
Q2012 turns off again midway in this discharging, and C2066 is charged. The level at pin 3 of IC2009 does not drop lower than the level at pin 4 in this operation and pin 2 becomes Lo. (FM AUTO: Lo).

The DO pulse width gets wider when an FM drop occurs.

| | C2066 (FM AUTO system) | | C2079 (LINE MUTE system) | |
|---|---|---|---|---|
| | Charge | Discharge | Discharge | Charge |
| Charge/ discharge circuit | R2052/ D2007 | R2051/ Q2012 | R2052/ R2082 | D2020/ Q2012 |
| Charge/ discharge time | Short | Long | Long | Short |

Taking into consideration the charge (Q2012 OFF) and discharge (Q2012 ON) of C2066 and C2079, the following relationship is established as shown in the table.
When the DO pulse width gets wider than the specified (FM output gets lower), the smoothing level at pin 3 is higher than the level at pin 4 (FM AUTO: Lo), but D2020 anode becomes Lo (LINE MUTE: Lo). Following these operations, the FM audio is played back or the output route is shut off by the line mute signal.

**Linear Audio Output**

When the FM drop becomes greater or the FM signal is not detected, the condition shown above advances further and the level at pin 3 of IC2009 gets lower than the level at pin 4. This causes the FM AUTO also to be Hi, and Hi-Fi output is changed over to linear audio output.
The Hi-Fi output has precedence in this system but the resistance of R2051 is greater, so when the FM drop occurs during playback, it takes approx. 1.2 seconds to switch over from Hi-Fi output to linear audio output.

**FM Audio Circuit Operation during Video Dubbing**

The FM audio circuit performs the following processing during video dubbing to improve the played back picture and sound.

- Shuts off the L-CH FM audio system (no-signal recording), and this section is forcibly set to the linear audio output caused by dropout of L-CH to remove discontinuity sound during play. However, when playback of the video dubbed section is entered, muting for 1.2 seconds is applied when Hi-Fi is changed to linear . . . . . L-CH audio system operates without recording a signal.
- Erases the prerecorded video using the R-CH FM audio signal, and records a new video just after it . . . . . R-CH audio is recorded with "current-up".

Fig. 5 shows the video dubbing control circuit.

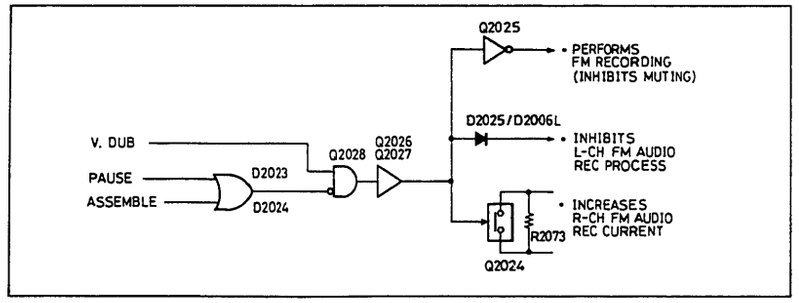



Fig. 5 Video Dubbing Control Circuit

The signal used to control the FM audio circuit during video dubbing is obtained by Q2026 and Q2027. Q2026 and Q2027 output Hi during video dubbing. However, they output Lo during video dub pause and in the assemble mode after the pause is released.
This signal:

- turns on Q2025 and grounds the "MUTE" line. This forms the recording process in the video dub mode and enables FM audio to be recorded,
- is supplied to the L-CH FM audio recording process via D2025/D2006L, and no signal is recorded by the L-CH system. This forcibly changes over to the linear audio play when playing this section.
- turns on Q2025 and short-circuits R2073. This lowers the impedance of the R-CH FM audio recording process and increases the recording current. This increased current records a new video signal while erasing the prerecorded video signal, so when playing back this section, pictures with less color noise (rainbow noise) can be obtained because of the multiplex effect with the "current-up" of the video record signal.

## VOLTAGE SYNTHESIZER CHANNEL SELECT CIRCUIT

### Outline

The voltage synthesizer channel select circuit used in this unit has the following functions.

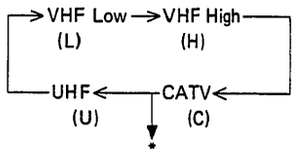
- 133 channels can be received and 80 positions can be preset for automatic tuning.
- The band, channel number and AFT ON/OFF can be checked from the ON Screen Display (OSD).
- Auto tuning preset by the search button.
- Signals transmitted from the IR remote control hand unit are decoded.

The voltage synthesizer channel select circuit converts the tuning voltage obtained by the conventional preset control to a code, stores it in the μP and selects a channel tuning the code. The μP increases the tuning voltage with the specified period during presetting. When the tuning point is reached, the μP stores the voltage, band, AFT ON/OFF and SKIP ON/OFF at this point. When a channel is selected, the μP reads the code of the tuning voltage corresponding to the selected channel number from the memory, converts it to the tuning voltage using the peripheral circuits and applies it to the local oscillator in the tuner circuit.

### Presetting Procedure

When the channel preset operation is advanced according to the flow chart shown below, the data concerning the tuned channel is stored in the μP.
Switch operations of the BAND, SELECT/NORMAL and " ∧ "/" ∨ " (on the VTR) are possible during search, and when these operations are performed, the following is obtained:

- When the BAND button is pressed: The search operation stops, the band shifts to the next band and the tuning data before starting the search operation is held.
- When the SELECT/NORMAL button is pressed: The search operation stops, the picture during search stopped appears and the data before starting the search operation is held.
- When the " ∧ " / " ∨ " button on the VTR is pressed: The channel indication changes and the search operation continues.

| Button Operation | Indication on monitor screen | Circuit Operation |
|---|---|---|
| Set the NORMAL/SELECT button to "SELECT" | The band, channel and condition of AFT are displayed. | Tuning Standby: The sequence for tuning is entered. |
| 〈Position (Channel) Set〉 | Ⓐ | |
| Select channel number to be preset | Indicated channel number changes. | The channel indication output is added/subtracted. |
| 〈Band Set〉 | | |
| Designate the band desired to be received by operating the BAND select button | The band is varied cyclically.<br>  | The band indication output is shifted in sequence. |



〈Search Operation〉

Press the SEARCH button for automatic channel search.

- The tuning voltage is boosted.
- Sound is muted.
- AFT is OFF during search.

〈When tuning point is preset〉

Press the SEARCH button again when the channel is different from that desired.

- The tuning voltage stops being boosted.
- Sound is output.
- AFT ON
- Data (channel number, band, AFT, SKIP) is stored in the EAROM.

〈When tuning point shifts a little〉

Detect the desired picture using the Tuning "∨"/"∧" button.

- AFT OFF
- Tuning data changes.
- AFT OFF, new tuning data is stored in the EAROM.

〈Skip Selection〉

Determine whether or not to skip the channel using the SKIP button when the channel will be selected.

The defeat output is controlled. The skip condition is stored in the EAROM.

〈Preset Complete〉

Return to loop Ⓐ when presetting another channel. Set the NORMAL/SELECT button to "NORMAL" when completing preset.

Band, channel number and AFT indications disappear from the screen.

The sequence for presetting is completed.

### 3. Circuit Configuration

Fig. 1 shows the configuration of the voltage synthesizer channel select circuit.
The channel select circuit has the C-MOS 4-bit μP (IC1701) as its center and is also composed of the data memory EAROM (IC1702), band selector (IC1704), tuning voltage generation smoothing circuit (RC integrating circuit centered on Q1702), timer μP (IC1201) and the timer display.
The channel select circuit has the following functions.

- Channel preset function
  4 types of data, turning voltage (13 bits), skip of unnecessary channels (1 bit), AFT (1 bit) and band (2 bits) are simultaneously stored as the preset data for each channel.
- The selected channel number is indicated in the timer display using the communication line with Time μP.
- The band, channel number and AFT ON/OFF are displayed on the monitor screen. (OSD)
  The data from Tuning μP is sent to Timer μP; and in the OSD mode, it is also sent to the character generator circuit.
- IF circuit defeat control and AFT control functions
- Band selection and tuning voltage generation
- Decoding of the IR remote input
  The decoding output is sent to System Control μP via Timer μP.

**EAROM: IC1702**

EAROM is the abbreviation for Electrically Alterable ROM, it is an electrically erasable and programmable ROM composed of 1400 bits (14 bits x 100 words).

The EAROM can control the "WRITE", "ERASE" and "READ" operations according to the levels at pins 7, 8 and 9, so the data input to Tuning $\mu$P is stored in IC1702 in sequence when presetting channels. When the channel number is designated to Tuning $\mu$P during channel selection, Tuning $\mu$P reads out the corresponding data rapidly from the EAROM to select the channel. Data read/write are done by synchronizing the data at IC1702 pin 12 with the clock (sent from the $\mu$P) at pin 6.

When the channel number is designated to Tuning $\mu$P, the $\mu$P converts it to a "1-OUT-OF-10" code. The address data (channel number) is divided into its 10's digit and unit's digit by this encoding method, and indicated serially. When the address data is determined, the other data is encoded in 14-bit units and transmitted.

Fig. 2 shows the data transfer timing chart between EAROM and Tuning $\mu$P. The operation of the EAROM control pin group of Tuning $\mu$P is shown in Table-A in "TUNING IC (IC1701) PIN SPECIFICATIONS".

An example of the timing between the address input and data output is shown in the figure. When the address input is commanded via C1 ~ C3, "CHANNEL 15" is transmitted

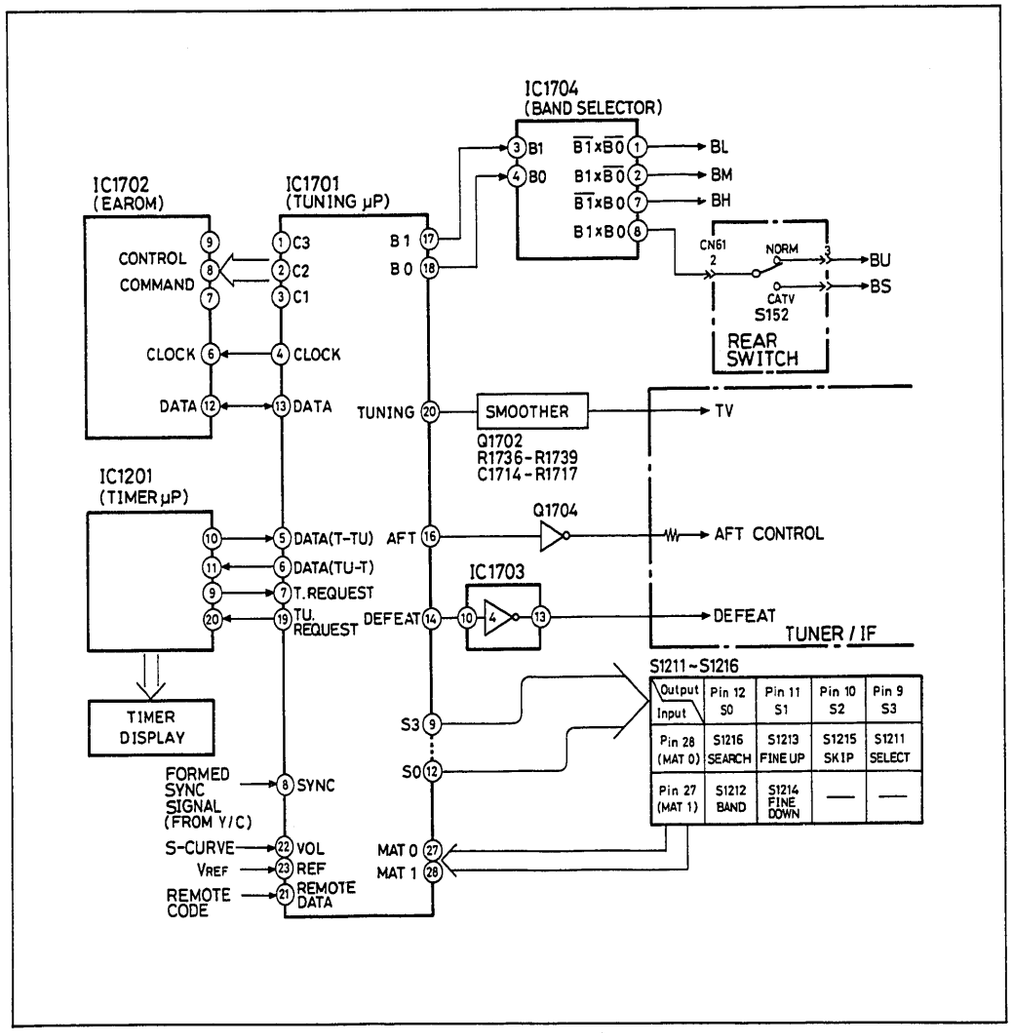



**Fig. 1 Voltage Synthesizer Channel Select Circuit Configuration**



to the EAROM from the $\mu$P synchronized with the clock pulse. When the data output is commanded via C1 ~ C3, the data is transferred in 14-bit units synchronized with the clock pulse. The serial data of "tuning voltage" "skip", "AFT", "band" are divided into 2 and transferred.

The 1st transfer is 14 bits and includes the tuning voltage (13 bits) and Skip (1 bit), and the 2nd transfer is 3 bits and includes AFT (1 bit) and Band (2 bits).

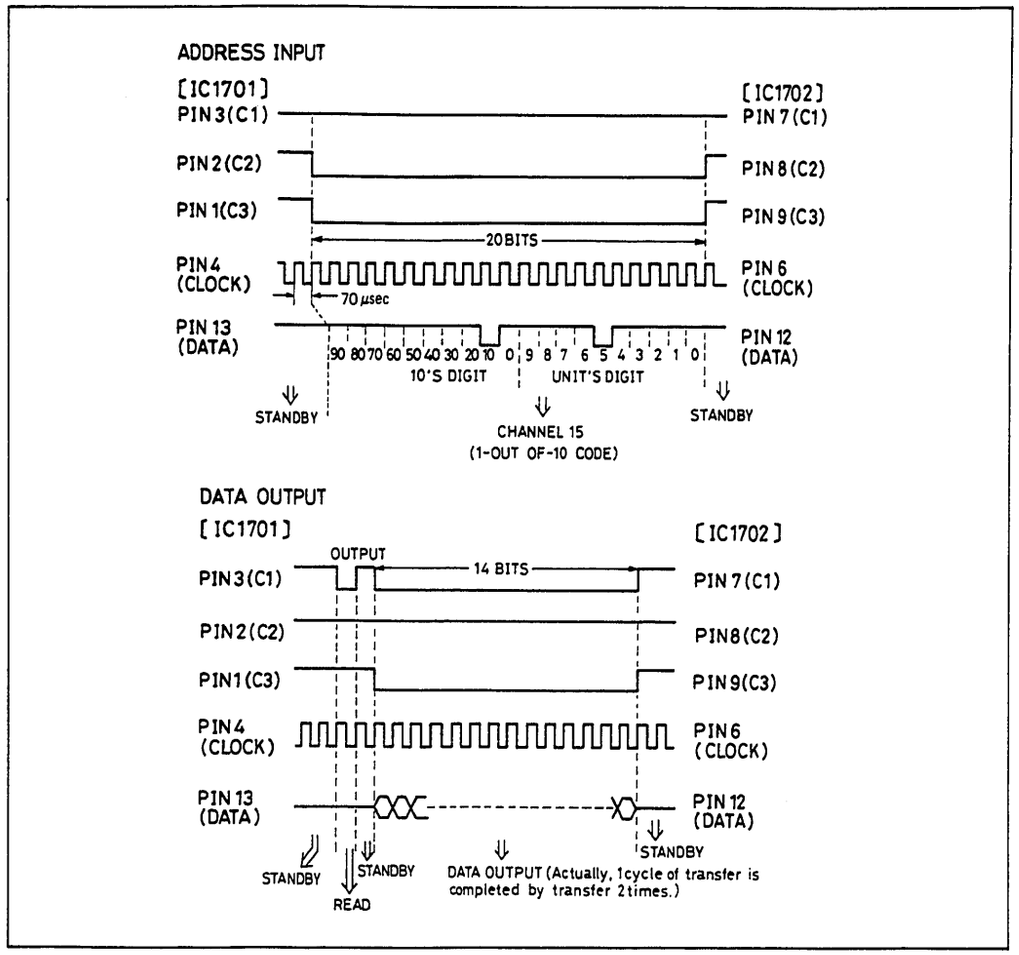



**Fig. 2 Tuning $\mu$P/EAROM Data Transfer Timing Chart**

**Timer $\mu$P: IC1201**

Timer $\mu$P has 4 communication lines (2 single direction data lines and 2 response lines) to Tuning $\mu$P, and it receives the data when selecting and presetting channels and the remote control operation data. Receiving this data, the Timer $\mu$P performs channel indication during channel selection and Band/channel/AFT indication during presetting and transfers the remote control operation mode to System Control $\mu$P.

**Band Selector: IC1704**

When selecting band UHF, VHF, etc., outputs from 2 lines (pins 17, 18) of Tuning $\mu$P are converted to 4 outputs by IC1704. IC1704 outputs band select voltages, VHF-Lo at pin 1, VHF-Hi at pin 2, CATV at pin 7 and UHF at pin 8. The table 1 shows the relation between input and output. The Boolean alegebra shown in the figure is established for the relation between the band selector input and output.

When the band select operation is performed,

Mute output pin 14 of Timing $\mu$P becomes Hi for approx. 90 msec and the IF circuit is defeated for this period.

AFT output pin 16 of Timing $\mu$P becomes Lo regardless of its condition up to that time, and the "AFT OFF" state is entered.

**Table 1 IC1704 I/O Table and Channel Selection**

| B1 PIN 3 | B0 PIN 4 | BAND | CHANNEL RECEIVED | CHANNEL NUMBER | IC1704 H: OUTPUT |
|---|---|---|---|---|---|
| Lo | Lo | VHF LOWER (54M – 88 MHz) | 2 – 6 | 2 – 6 | PIN 1 |
| | | VHF LOWER MID (90 – 120 MHz) | A5 | 69 | |
| Hi | Lo | | A4 – A1 | 70 – 73 | PIN 2 |
| | | VHF UPPER MID (120 – 174 MHz) | A – I | 14 – 22 | |
| Lo | Hi | VHF UPPER (174 – 216 MHz) | 7 – 13 | 7 – 13 | PIN 7 |
| | | SUPER (216 – 300 MHz) | J – 0 | 23 – 28 | |
| Hi | Hi | | P – W | 29 – 36 | PIN 8 |
| | | HYPER (300 – 438 MHz) | W+1 – W+26 | 37 – 62 | |
| | | UHF (470 – 890 MHz) | 14 – 83 | 14 – 83 | |

**Key Matrix: S1211 ~ S1216**

Switches for presetting channels are located as shown in Fig. 1. When S3 pulse is applied to pin 28 using S1211 (SELECT switch), the key operation becomes effective and tuning is possible.

| Output / Input | Pin 12 S0 | Pin 11 S1 | Pin 10 S2 | Pin 9 S3 |
|---|---|---|---|---|
| Pin 28 (MAT 0) | S1216 SEARCH | S1213 FINE UP | S1215 SKIP. | S1211 SELECT |
| Pin 27 (MAT 1) | S1212 BAND | S1214 FINE DOWN | – | – |

## Search Operation

When the Select/Normal switch is set to "SELECT", presetting becomes possible and the tuning $\mu$P accepts the search switch (S1216) operation. When the search key is pressed, the $\mu$P sets pin 14 (DEFEAT) to Hi and pin 16 (AFT) to Lo.

Refer to the timing chart.

The sweep-up operation is determined by the state of the sync detection terminal pin 8 and the state of the IF-S curve at pin 22. Hi is applied to pin 8 from the external sync detection circuit when a broadcast is detected, and the "S" curve voltage is applied to pin 22 from the IF circuit; the tuning $\mu$P discriminates the tuning point from the state of this curve.

2 operational amplifiers are built into pin 22, and the state of the "S" curve is judged via the reference voltage ($V_1$) determined by pin 23 and its 2 times voltage ($V_2$) determined accordingly. The operational amplifiers generate the Up signal and Down signal from the "S" curve and control the sweeping condition in the $\mu$P. The "S" curve has been detected by pins 22, 33, so the sweep-up operation changes in the following 6 modes (MODE 0 – MODE 5) based on this "S" curve. Table 2 shows the number of steps in each mode and the total number of steps.

| Mode | Operation & Purpose | Detection Method (Circuit Operation) |
|---|---|---|
| MODE 0 | Sweeps up in 8 steps to detune from the present station. | Detects detuning with pin 8 set to Lo and the UP signal to Lo. |
| MODE 1 | Sweeps up in 8 steps to detect the next station. | Detects the rise of the "S" curve with pin 8 set to Hi and the UP signal to Hi. |
| MODE 2 | Sweeps up by 1 step to detect the tuning point of the detected station. | Detects the fall of the "S" curve with the UP signal set to Lo and the DOWN signal to Lo. |
| MODE 3 | Sweeps down by 1 step to the tuning point. | Sweeps down until the rise of the UP signal is detected. |
| MODE 4 | Sweeps up by 1 step to the tuning point. | Sweeps up until the rise of the DOWN signal is detected. |
| MODE 5 | 30 (VHF Lo)<br>20 (VHF Hi, CATV)<br>5 (UHF) } | Steps down |

When the tuning point is detected,
- AFT ON: Pin 14 Lo,
- DEFEAT: Pin Lo,

and presetting is complete.



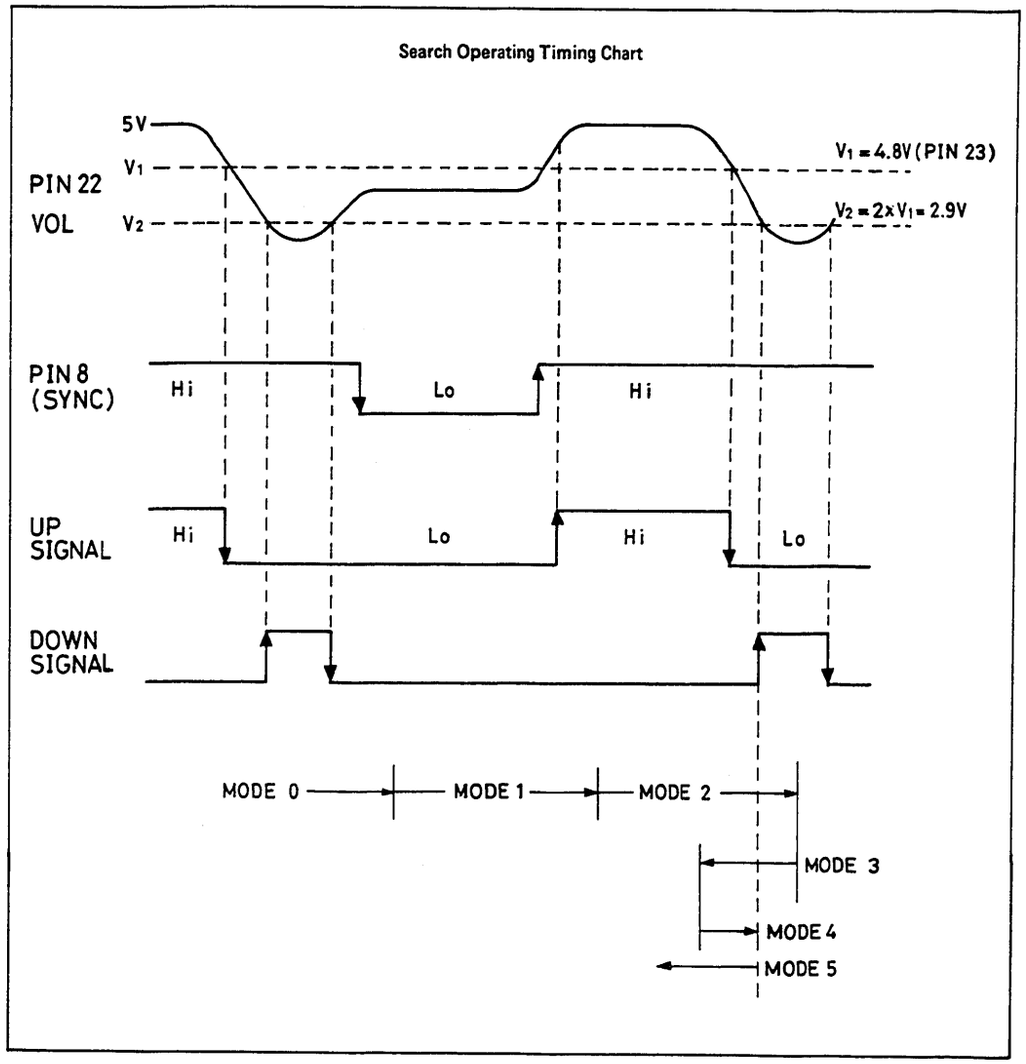



**Table 2 Number of Steps and Sweep Time during Search**

(Sweep Time means the time required to sweep up from lower end to upper end with the number of steps in each mode.)

| Mode / Band | Steps required for detuning when search starts. | Modes 0, 1 | | Modes 2, 3 | | Mode 4, Fine tune | |
|---|---|---|---|---|---|---|---|
| | | Number of steps each time | Sweep time | Number of steps each time | Sweep time | Number of steps each time | Sweep time |
| VHF-L | 256 | 8 | 4.4 sec. | 1 | 65.5 sec. | 1 | 131 sec. |
| VHF-H | 128 | 8 | 8.8 sec. | 1 | 130.7 sec. | 1 | 260 sec. |
| CATV | 128 | 8 | 8.8 sec. | 1 | 130.7 sec. | 1 | 260 sec. |
| UHF | 64 | 8 | 16.1 sec. | 1 | 260 sec. | 1 | 528 sec. |

## SERVO CIRCUIT

### Outline

The configuration of the servo circuit in this unit is the same as that in portable VTR VT-7 except for the following.

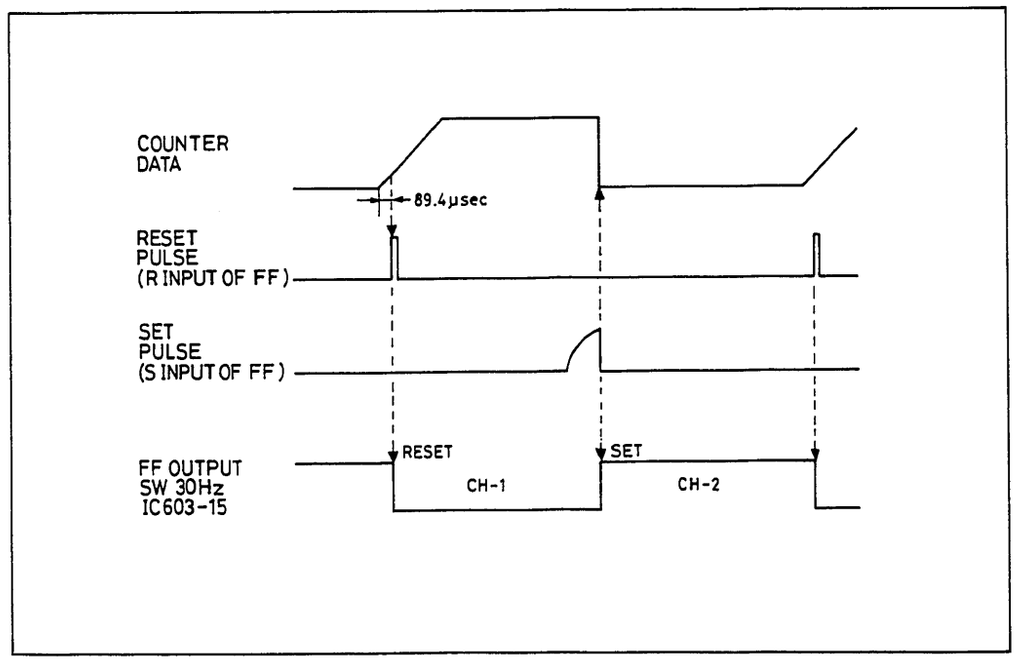
- The divider (IC602) installed in the route of the CFG pulse and CTL pulse is made to correspond with double speed play and LP trick play to enable quick play and LP trick play.
- The circuit configuration such as pretracking and switching point, etc. differs to correspond with various trick play modes including double speed play.
  The slow speed is set to 1/5 at max. regardless of the tape speed.
- Number of frames advanced when entering the still mode is changed to 3 frames from the previous 5 frames so that the unit can enter the still mode more quickly.

### SW30 Hz Pulse Generation

The head switching SW 30Hz pulse is obtained from IC603 pin 15 as the pulse with a duty of 50%. This circuit is composed of the tack pulse monostable multivibrator, counter and RS-FF.

Refer to the SW30 Hz generation timing chart.
The counter reset by the CH-1 MM output starts counting the clock pulses.
The counter generates the pulse used to reset the RS-FF after 89.4 μsec, and this becomes the trailing edge of the SW30 Hz pulse. This pulse sets the FF output to Lo. The CH-2 MM output generates the pulse which sets the RS-FF. The SW30 Hz pulse is generated via this process.
The CH-1 edge and CH-2 edge of the SW30 Hz pulse can be varied by the time constant circuits, connected to pins 13 and 12, of respective MMs, and the pulse duty is adjusted to 50% regardless of the operation mode.
Fig. 1 shows the SW30 Hz pulse phase control circuit.
The CH-1 edge can be adjusted by 2 semi-variable resistors:
RT612: EP CH-1 phase
RT614: SP CH-1 phase
The CH-2 edge can be adjusted by 3 semi-variable resistors:
RT611: EP CH-2 phase
RT613: SP CH-2 phase
RT616: Reverse search switching point
The resistor composition as shown in the table is obtained corresponding to the tape speed and operation mode detecting the signal which selects each resistor.

**SW30 Hz Generation Timing Chart**





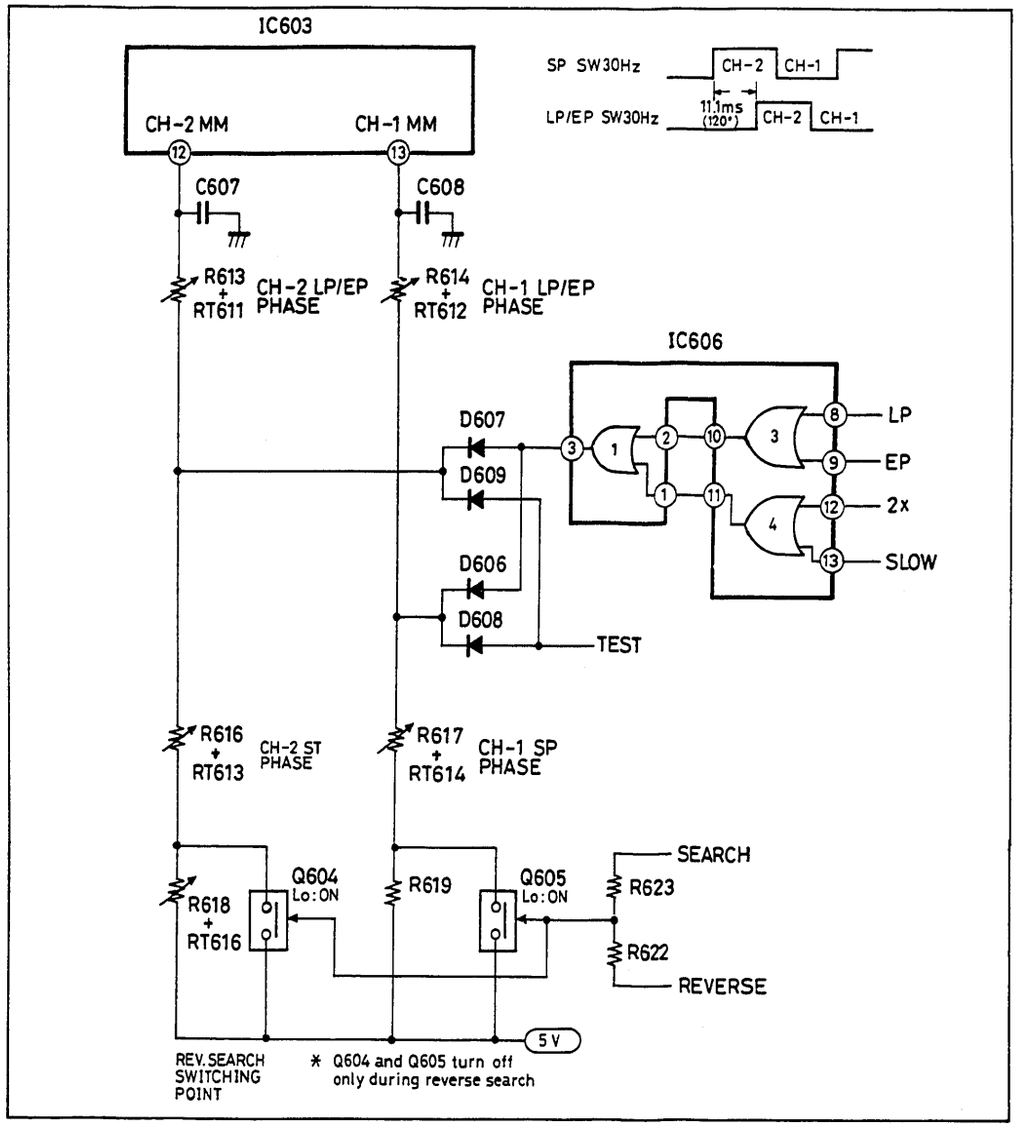




**Fig. 1 Switching Point Control Circuit**

**Table 1 Switching Point Resistor Composition**

| Mode \ Tape Speed | | SP | EP/LP |
|---|---|---|---|
| Normal Processing, Forward Search, Reverse Play | CH-1 | R614+RT612+R617 +RT614+R619 | R614+RT612 |
| | CH-2 | R613+RT611+R616 +RT613+R618+RT616 | R613+RT611 |
| Reverse Search | CH-1 | R614+RT612+R617 +RT614 | Same as in normal play |
| | CH-2 | R613+RT611+R616 +RT613 | " |
| Slow, Still, Frame Advance | CH-1 | R614+RT612 | " |
| | CH-2 | R613+RT611 | " |

## CFG Pulse Route

Refer to Fig. 2.
The CFG pulse obtained from the FG (Frequency Generator) of the capstan motor is applied to IC602 pin 2. IC602 incorporates a divider and outputs the divided CFG pulse at pin 4. The division ratio is 1/15 in EP search, 1/9 in LP search, 1/5 in SP search, 1/2 in double speed play and 1 in normal play, and the output frequency is 2160 Hz in the SP mode, 1080 Hz in the LP mode and 720 Hz in the EP mode. The output from pin 4 is input via pin 32 to IC604. Speed control is done in IC604 by this CFG pulse. This CFG pulse is divided by 3 in IC604, is output from pin 30 and supplied via pin 6 to IC603 to operate the capstan phase control system during recording.
The CFG pulse (720 Hz in SP, 360 Hz in LP and 240 Hz in EP) at IC603 pin 6 is phase compared with the REF 30 Hz output from the built-in REF counter during recording to control the capstan phase.

## Capstan Speed Control

The capstan speed control system operates basically the same as that in the conventional VT-7, but functions such as LP search and quick play, etc. are added, so operations in the modes shown above are slightly different.
Fig. 2 shows the capstan speed control system.

The CFG pulse (2160 Hz in SP mode, 1080 Hz in LP mode, 720 Hz in EP mode) supplied via pin 32 to IC604 is divided by the internal counter (1/3 division in SP and 1/1 division in LP/EP) and is fed to the pulse generator. The pulse generator generates the counter reset pulse and counter data latch pulse using the divided CFG pulse.
In the capstan speed control system, the counter, after being set by the reset pulse, counts the continuously input clock pulses, and performs the counter operation for every period of the CFG pulse. The counter data is held every period by the latch pulse. The PWM wave is obtained from this data, and the PWM wave is converted to an analog value to be the capstan speed control signal. This is added to the phase control signal input via pin 26 and output at pin 28. Speed control is performed by varying the bias level at pin 27 using RT607 connected to pin 27 and adding it in DC to the speed control output.
Refer to the capstan speed control timing chart.
The CFG pulse changes depending on the capstan speed in each operation mode and its frequency is set as follows.

SP normal recording/play: 2160 Hz
SP x 5 speed search: 10800 Hz
LP normal play: 1080 Hz
LP x 9 speed search: 9720 Hz
EP normal recording/play: 720 Hz
EP x 15 speed search: 10800 Hz

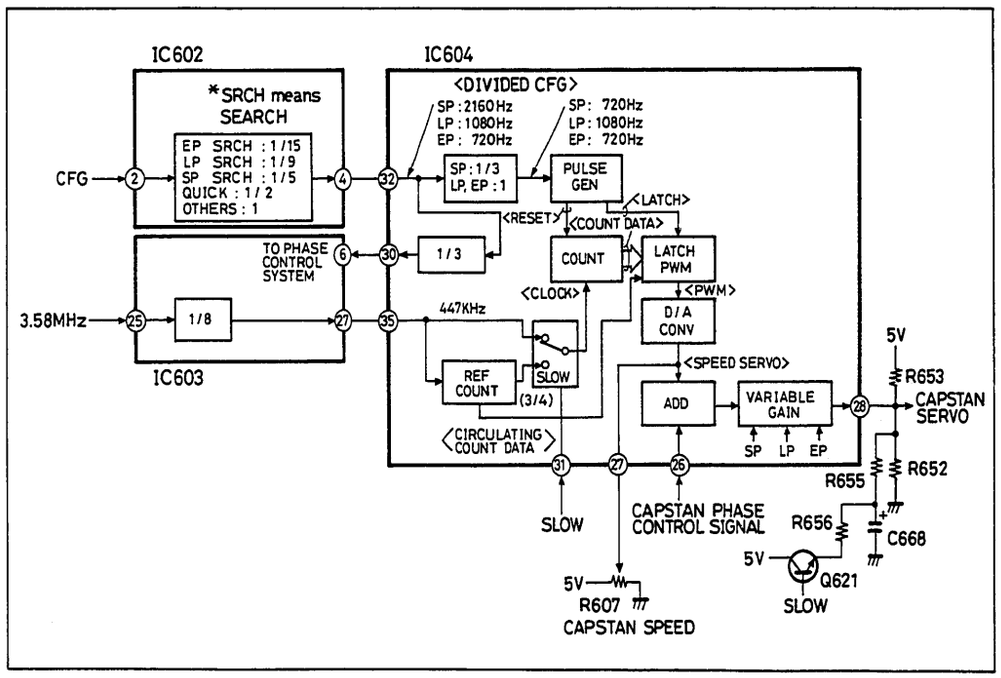
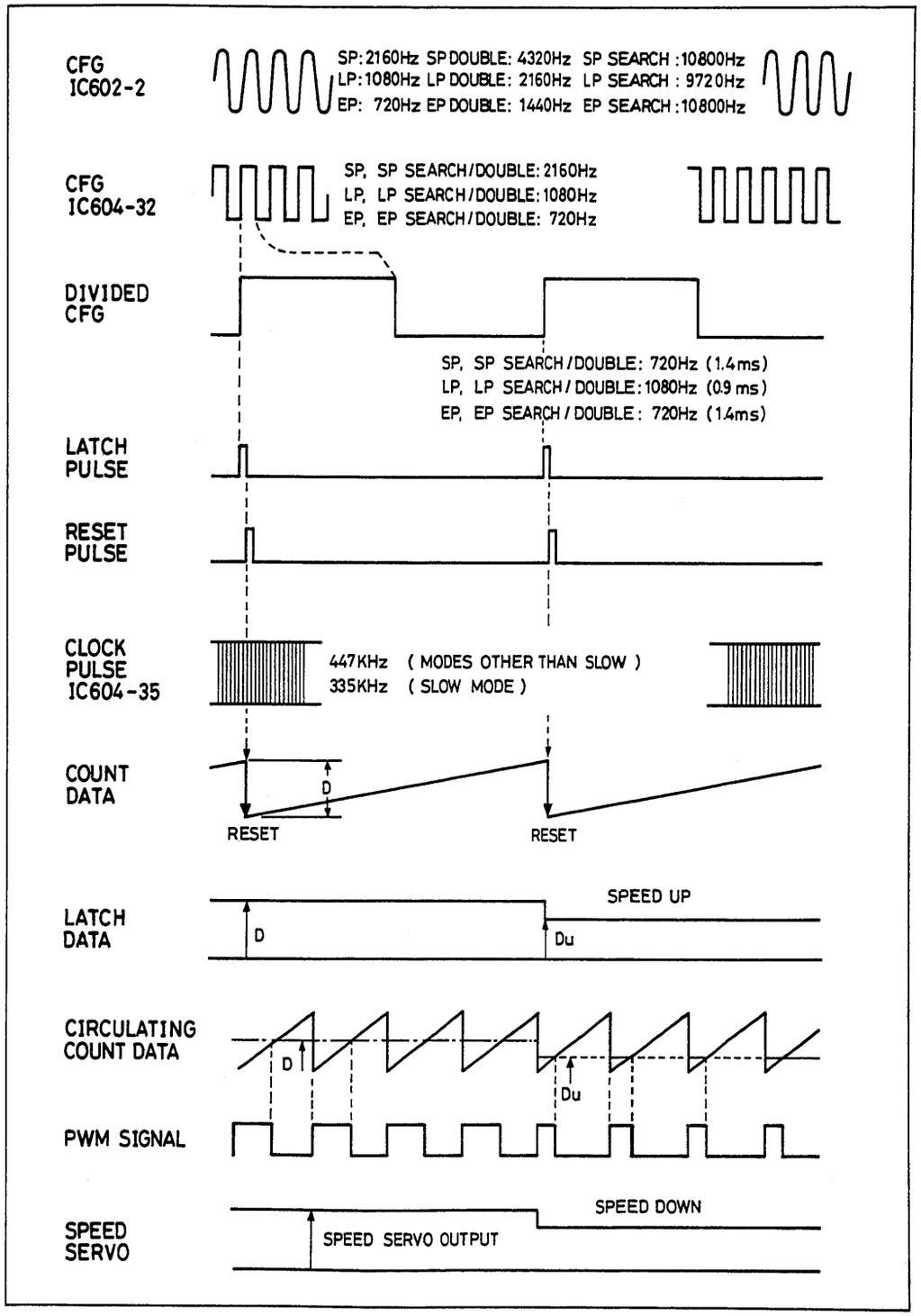



Fig. 2 Capstan Speed Control System



Capstan Speed Control Timing Chart



The CFG pulse is supplied via pin 2 to IC602 and divided. The divider in IC602 operates as follows so that the CFG pulse used for the speed control system is set constant regardless of the operation mode for all tape speeds (SP, LP, EP).

- 1/15 division in EP search
- 1/9 division in LP search
- 1/5 division in SP search
- 1/2 division in double speed play
- No division in other modes

(Refer to "variable divider operation" in "CTL Pulse Recording/Playback Route" described later for the division ratio of this variable divider.)

The frequency of the CFG pulse obtained in IC602 is as follows:

SP standard record/play, search: 2160 Hz
LP standard record/play, search: 1080 Hz
EP standard record/play, search: 720 Hz

The CFG pulse is supplied via pin 32 to IC604. The CFG pulse at pin 32 is previously divided by 3 in IC604 only in the SP mode to lower the capacitance of the counter in the speed control system. The frequency of the pulse obtained in this way is 720 Hz in the SP/EP modes and 1080 Hz in the LP mode. Two pulses are produced from this divided CFG pulse by means of the pulse generator in the next stage. One is the reset pulse used to reset the counter every period of the CFG pulse to start counting, and the other is the latch pulse used to read the count data every period of the counter. The counter is operated by these pulses and converts the latch data to the PWM wave with the PWM generator.

The counter starts counting the clock when it receives the reset pulse. The clock is the 447 kHz pulse obtained when the 3.58 MHz signal sent from the Y/chroma system is divided by 8 in IC603, and is supplied to the switch and REF counter in IC604. In the REF counter, 3/4 division is performed to obtain the clock pulse for the slow mode. The 3/4 divided clock pulse 335 kHz is fed to the switch, the same as the 447 kHz clock pulse, and is switched over by the voltage at pin 31.

The REF counter always generates the circulating count data from the clock pulse to perform pulse wave modulation (PWM).

PWM is the operation to mudulate the circulating count data fed from the REF counter with the latch data and to generate a pulse with the width corresponding to the latch data.

When the capstan speed increases, the period of the CFG pulse becomes smaller and latch data gets smaller. This causes the duty of the PWM wave to be smaller, and the analog conversion value becomes low. As a result, the motor speed decreases. When the motor speed increases, the reverse operation is performed. The motor speed is driven to the target value by these operations.

#### Operation during slow play

The "SLOW" signal is supplied from System Control μP during slow play. This signal:

- is supplied to pin 31 and switches over the clock frequency during slow play,
- activates Q621, varies the bias level at pin 28 and sets the feed rate speed of the capstan motor to 3/4.

### Capstan Phase Control

Fig. 3 shows the capstan phase control system.

The CTL pulse supplied via pin 21 to IC603 and the CFG pulse which is supplied to pin 6 and divided to 30 Hz in IC603 are selected by the record/play switch and fed to the latch circuit as the latch pulse. In the latch circuit, the phase difference from the reference signal is counted digitally. The reference signal is produced by dividing the 3.58 MHz signal applied via pin 25 to 30 Hz in the REF counter, and is supplied to the counter circuit to measure the phase difference from the comparison signal.

The REF30 Hz signal is directly supplied to the counter as the reset pulse during recording. In the play mode, it is delayed by the monostable multivibrator for tracking control and then supplied as the reset pulse. The counter is reset by the REF30 Hz pulse and starts counting the clock pulses. It holds the count amount by the latch pulse to use it as the phase difference data.

The 3.58 MHz pulse supplied to pin 25 is divided by 8 and becomes the 447 kHz clock pulse. The pulse becomes the reference signal for the servo system operation, and is fed to the REF counter and the phase difference detection counter. In the REF counter, this clock pulse is divided to 30 Hz to generate the REF 30 Hz signal. At the same time, the circulating count data is generated to obtain the phase difference as the PWM signal.

"REC: Hi" is applied to pin 7 when the servo circuit receives the data from the system control during recording, and the switch in IC603 is changed over to the REC position. The REF30 Hz signal is directly supplied to the counter as the reset pulse, and the divided CFG30 Hz pulse is selected as the latch pulse.

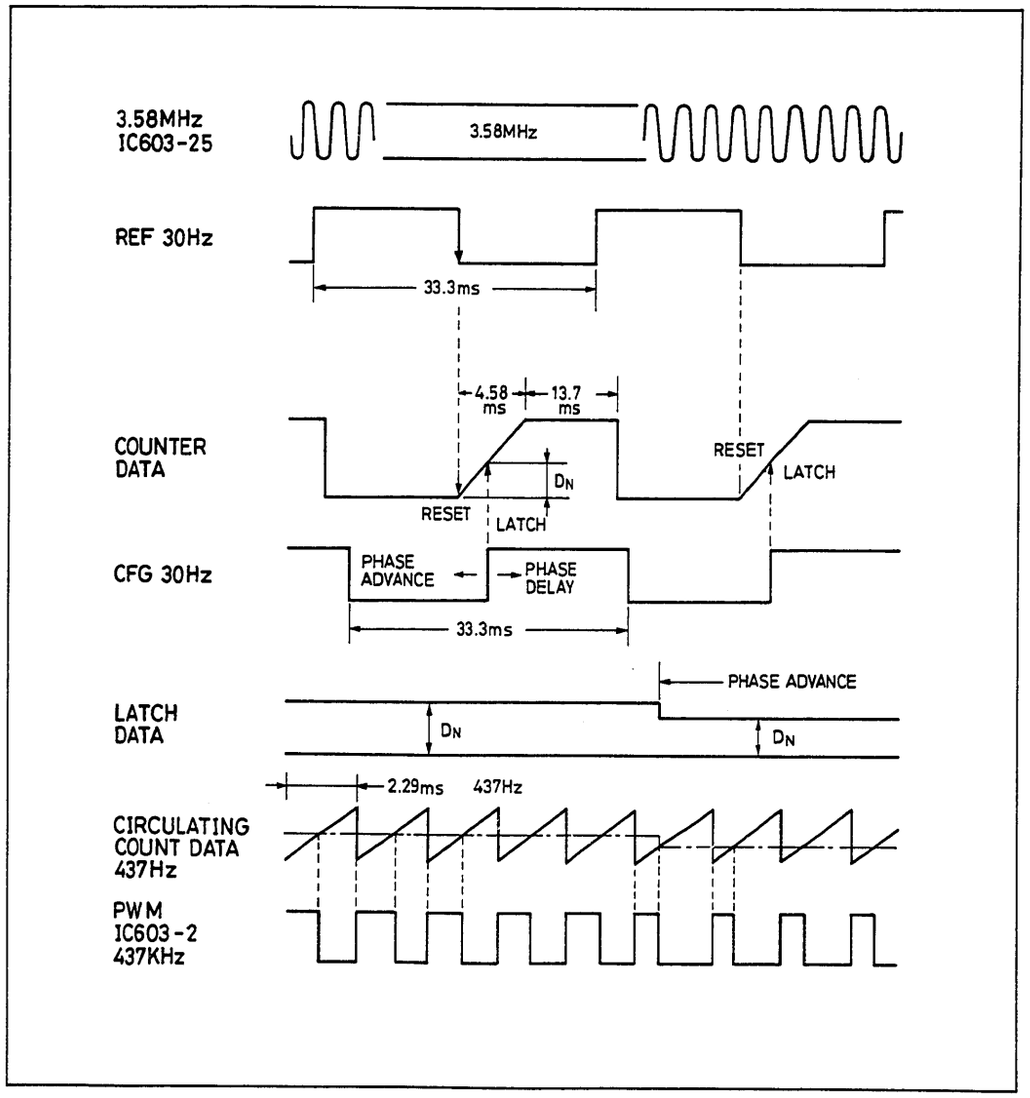
When the counter is reset at the trailing edge of the REF30 Hz signal, the counter starts counting the clock pulses. This count period is completed in 4.58 msec due to the counter capacitance, and then the counter output becomes Lo again 13.7 msec after completion. Sampling is performed by the CFG pulse in this 4.58 msec period. That is, the CFG pulse (refer to "CFG Pulse Route" for the route of the CFG pulse from the FG output) divided by 3 in IC604 is supplied via pin 6 to IC603 and divided to be 30 Hz.

The leading edge of this pulse becomes the latch pulse which samples the counter output. The circulating count data (437 Hz) fed from the REF counter is modulated by the above-mentioned latch data in the PWM generator in the next stage, and the PWM wave is obtained at pin 2. This PWM wave has 50% duty in the normal phase, but when the phase advances, the previous data is sampled and the duty becomes lower. The average value decreases and the motor is controlled so that the phase is delayed or the normal phase is restored. When the phase is delayed, the motor is controlled by the reverse procedure so the normal phase is restored.

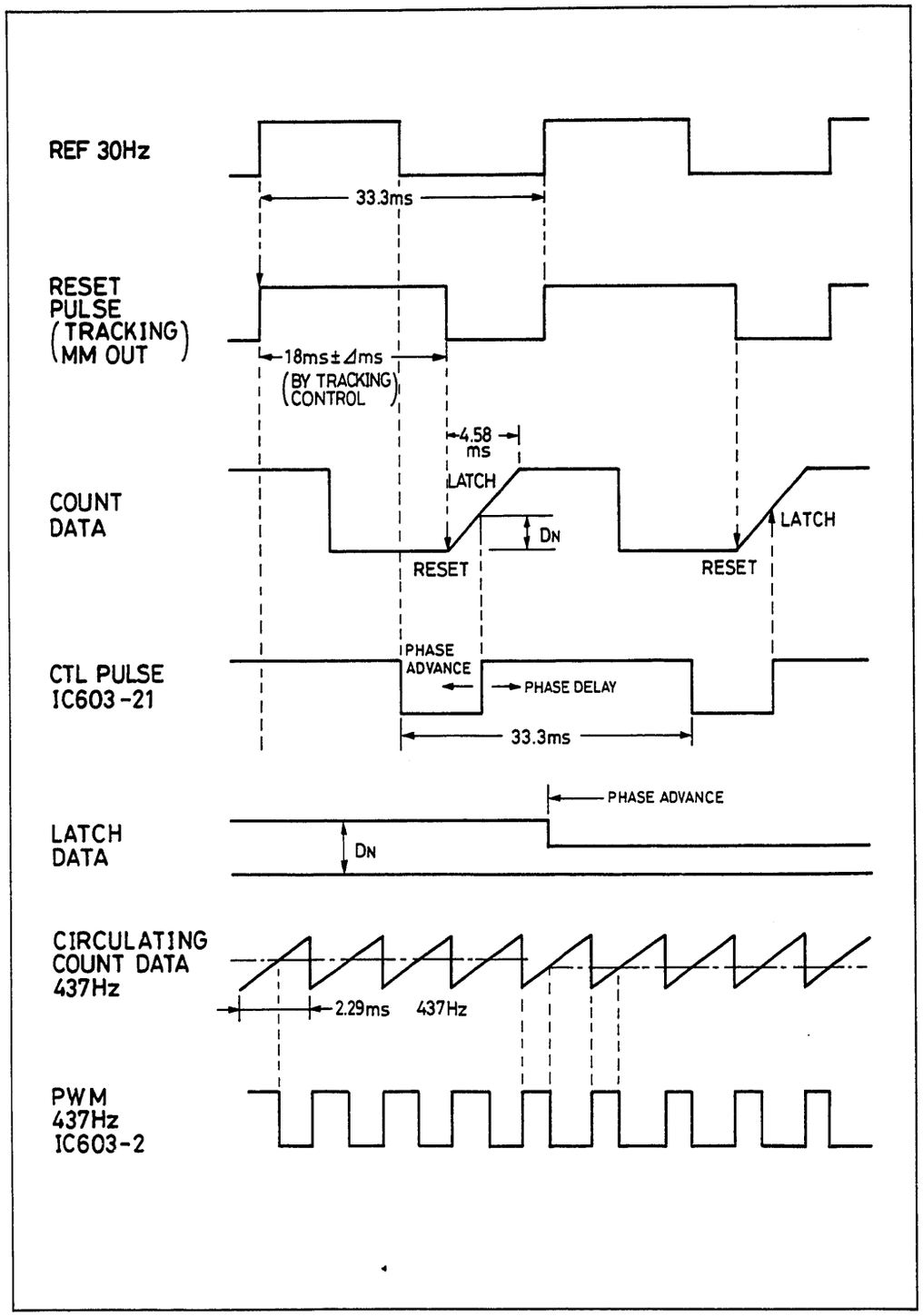
Since pin 7 is Lo in the play mode, the switch in IC603 is changed over to the play position. Therefore, the REF30 Hz pulse is adjusted by the tracking monostable multivibrator and works as the reset pulse. The latch operation is performed by the CTL pulse (refer to "CTL Pulse Recording/Playback Route" for the previous route of the CTL pulse) applied to pin 21. This CTL pulse is divided by the monostable multivibrator regulated by pin 22 in the search mode, but in this unit, the time constant of this MM is made smaller so that the division operation cannot be done. (It is not required in this unit because a search control circuit is provided.)

Tracking control is performed by the tracking control RV852 and the preset controls RT609 and RT610. The tracking amount is 18 msec ±Δmsec, and Δmsec is varied by the tracking control. To preset the tracking, RT609 is used in the LP/EP modes and RT610 is used in the SP mode. Sampling operation (phase comparison) using the CTL pulse and REF30 Hz plse is the same as in the record mode.

**Capstan Phase Control System Recording Timing Chart**



**Capstan Phase Control System Playback Timing Chart**





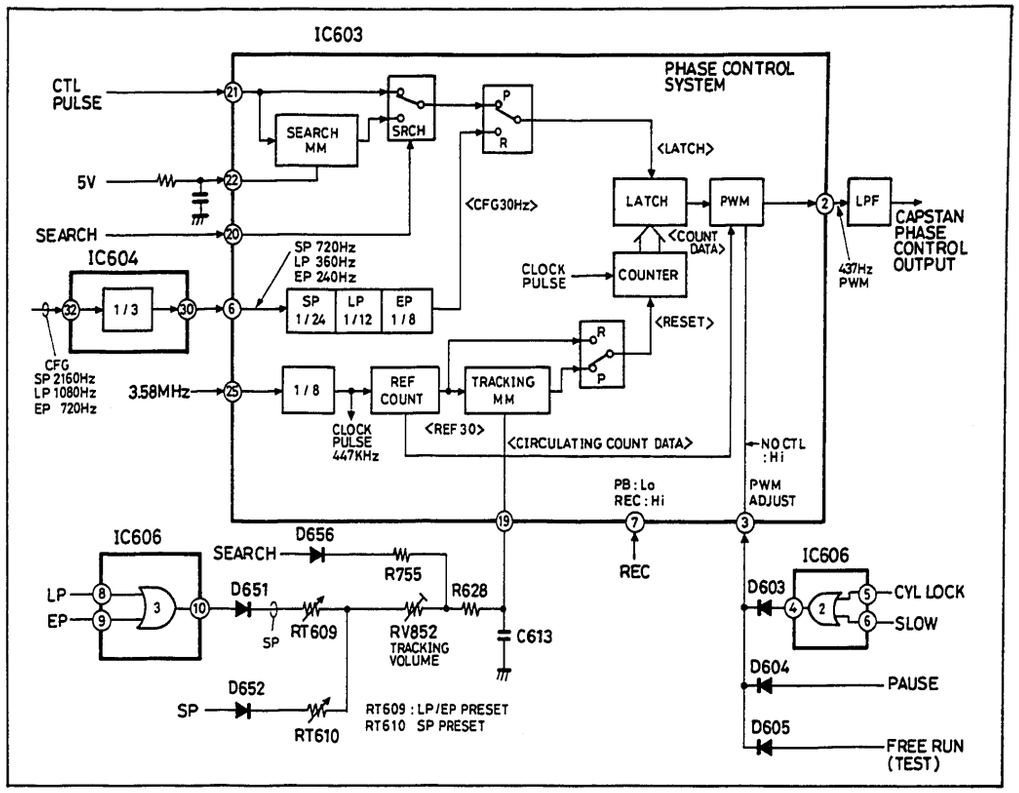




**Fig. 3 Capstan Phase Control System**

**Operation stop of capstan phase control system**

The capstan phase control system stops operating in the following cases.

- When the cylinder stops due to trouble
- During pause mode
- During slow play
- During no signal tape play

When Hi is applied to pin 3, the PWM wave generator fixes the PWM duty to 50%. This causes the phase control operation to stop. The cylinder lock signal detected by IC604 and the pause and slow signals output from the system control circuit are OR-input to pin 3 via inverter-2 in IC606, D603, D604 and D605. The phase control operation is not performed when these signal are input. The fact that there is no CTL pulse is detected by IC603 when a tape without a signal is played, and pin 3 is set to Hi to stop the phase control operation.

## CTL Pulse Recording/Playback Route

The comparison signal in the playback capstan phase control system and the playback CTL pulse which is used to generate the brake pulse for the intermittent drive during slow play are obtained when the vertical sync signal divided by 2 and recorded on the tape is played back.
Fig. 4 shows the control pulse recording/playback route. Recording and playback are described separately in the following.

### CTL pulse record route

The CTL pulse is obtained when the vertical sync signal used in the cylinder phase control system is divided by 2 and recorded on the control track by the CTL head. The composite sync signal obtained in the Y/chroma system is, with its horizontal sync signal removed by the LPF composed of R625, R626, C614, C615, supplied via pin 17 to IC603 as the vertical sync signal. This signal is divided by 2 in the sync separator (VSS) circuit and becomes a 30 Hz pulse. Since IC603 changes over the built-in switch to the record side using the input to pin 7 in the record mode, this pulse is output at pin 18 via the record start control switch in the next stage and supplied via pin 21 to IC601.
The record start control switch is opened/closed by the "PAUSE" signal applied to pin 11, and is open during the pause mode so that the record CTL pulse does not flow to pin 18.
Since the built-in switch has been changed over to the record side by the input to pin 9, the pulse entering IC601 is output at pin 18 via MM1/MM2/MM3. A switch which is controlled by the input to pin 2 is installed before pin 18; it works to prevent the record CTL pulse from flowing to the head during phase matching and loading. In the record mode, the pulse is written on the tape by the head as the record pulse.

### CTL pulse play route

The CTL pulse detected by the CTL head is applied via pin 38 to IC604, amplified and output at pin 42. This pulse is supplied via pin 1 to IC602 and fed to the divider. This divider performs the following division operations and keeps the frequency of the CTL pulse applied to pin1 at 30 Hz.

- 1/15 division in EP search
- 1/9 division in LP search
- 1/5 division in SP search
- 1/2 division regardless of the tape speed in double speed play
- No division during normal play

The CTL30Hz pulse obtained in this way is output from IC602 via pin 3 and supplied via pin 3 to IC601.
The CTL pulse entered IC601 via pin 3 passes through MM1, MM3, reverse switch and REC/PB switch, and is output at pin 21 and supplied to IC603 via pin 21.
These MM1~MM3 do not perform the delay operation during normal play.
During playback, the CTL pulse input via pin 21 to IC603 and the REF30Hz pulse generated by the built-in REF counter are phase compared to control the capstan phase.

### Divider input level switching in visual search

In the visual search mode in which the tape speed is high, the playback CTL pulse output is higher than usual, so the bias level is switched according to the divider input to prevent erroneous division of the noise component. The method to switch R668 and R730 around IC602 pin 1 using D625, D624 and Q624 is used in this operation, and it is as shown below depending on the tape speed.

Forward Search

IC602 pin 13: Hi → Q624: ON → R730 grounded
: Division threshold level of the CTL pulse is made lower.
Note: IC602 pin 13 outputs Hi only in forward search to correct capstan search.

Reverse Search

IC602 pin 13: Lo Q624: OFF
REVERSE: Hi → D625: ON
SEARCH: Hi → D624: OFF
→ R668: Connected → Division threshold level of the CTL pulse is made higher.
Note: It is required to invert the threshold level to invert the CTL pulse in IC602 during reverse search.

### Artificial CTL pulse generation during play pause

When the play pause operation is done using a tape without the CTL pulse, the tape does not stop because the signal for pause timing is not present. An artificial CTL pulse is required to stop the tape without CTL pulses. Q606 and Q607 connected to IC602 pin 1 comprise the circuit used for this purpose, and it generates the artificial CTL pulse just after the play pause operation is done. The reference input signal is "SLOW" generated from System Control μP, and this signal becomes Hi during slow, still, (plays pause) and frame advance. The "SLOW" signal is supplied to Q606 and via pin 10 to IC602 and the artificial CTL pulse is generated at the output of Q606 according to the following procedure.
When the play pause mode is entered, IC602 pin 7 picks up the CTL pulse and outputs Hi. Q606 outputs Hi because of the "SLOW" signal a certain period after the play pause operation is done. When this Hi is applied via pin 1 to IC602, the leading edge of this pulse is assumed to be the

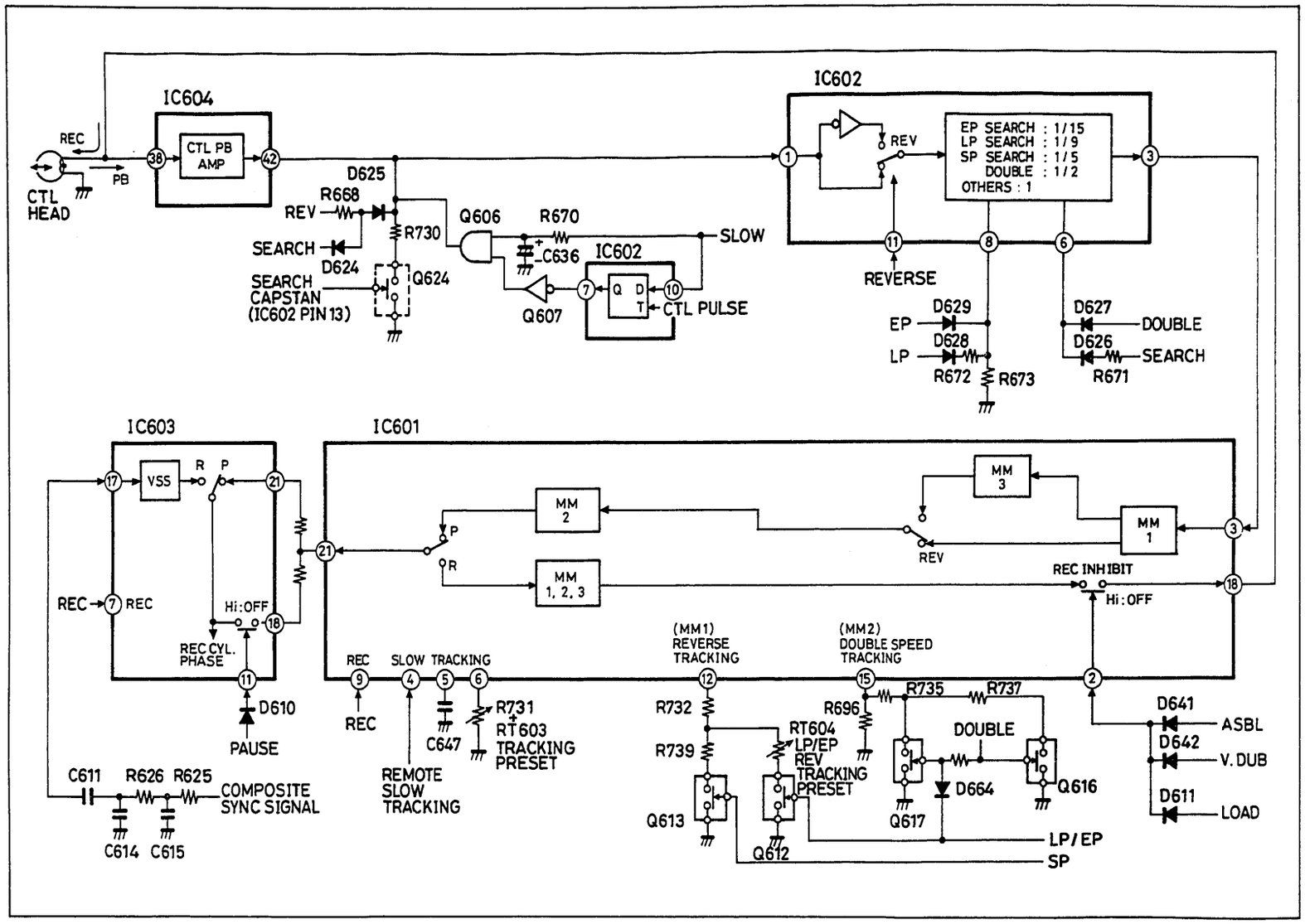



**Fig. 4 Control Pulse Recording/Playback Circuit**

CTL pulse and pin 7 is set to Hi. This causes Q607 to output Lo and Q606 to turn off. The integration circuit composed of R670 and C636 is installed to check the presence/absence of the CTL pulse in this operation just after the play pause is entered. The "SLOW" signal is delayed for a certain period by this circuit and supplied to Q606.

**Variable Divider Operation**

The variable divider is installed in the CTL pulse playback system and the CFG pulse route of IC602 so that noise lock visual search can be performed. The division ratio of this divider is determined by the DC level at pin 6 and pin 8. The division ratios during normal play and double speed play are determined by the level at pin 6; during visual search they are determined by the level at pin 8. This is as shown in the following table.

| Mode | Pin 6 | Pin 8 | Division Ratio |
|---|---|---|---|
| SP/LP/EP Normal Play | Lo | — | 1/1 |
| SP/LP/EP Double Speed Play | Hi | — | 1/2 |



| Mode | Pin 6 | Pin 8 | Division Ratio |
|---|---|---|---|
| SP Search | Mid | Lo | 1/5 |
| LP Search | Mid | Mid | 1/9 |
| EP Search | Mid | Hi | 1/15 |

**Tracking Control**

Tracking control during normal play and visual search is done by the time constant circuit connected to IC603 pin 19. Tracking control during slow, reverse play and double speed play is performed by controlling the delay of the CTL pulse play system in IC601. Slow tracking can be controlled by the time constant at pins 4, 5, 6, the reverse play tracking by the time constant at pin 12, and the quick play tracking by the time constant at pin 15.

**[Slow tracking control]**

The remote control tracking signal is supplied to pin 4 from the remote control decoder, and the presetting circuit is connected to pin 6. Slow tracking control is performed by the circuits connected to these 2 pins and the capacitance at pin 5.

**[Reverse play tracking control]**

The preset circuit is connected to pin 15 and presetting can be done at all tape speeds.

- Q613 turns on in the SP mode and (R732 + R739) becomes effective,
- Q612 turns on in the LP/EP modes and (R732 + RT604) becomes effective.

**[Double speed play tracking control]**

The preset circuit is connected to pin 15 and presetting can be done at all tape speeds.

- Q616 turns on in the SP mode and ( (R735 + R737)// R696) becomes effective.
- Q617 turns on in the LP/EP modes and (R735//R696) becomes effective.

## Visual Search

In the VT-89, phase control is done for the capstan motor in the search mode to perform noise lock search in which noise does not flow.
Relation between the tape speed and search speed, CTL pulse and CFG fryquency are shown in Table 2.

**Table 2 Search Speed in each Mode**

| Required Value / Mode | Search Speed | Tape Speed (cm/sec) | CTL Pulse (Hz) | CFG Pulse (Hz) |
|---|---|---|---|---|
| SP Normal Play | (x1 speed) | 3.335 | 30 | 2160 |
| SP Search | x 5 speed | 16.675 | 150 | 10800 |
| LP Normal Play | (x1 speed) | 1.668 | 30 | 1080 |
| LP Search | x 9 speed | 15.008 | 270 | 9720 |
| EP Normal Play | (x1 speed) | 1.112 | 30 | 720 |
| EP Search | x15 speed | 16.675 | 450 | 10800 |

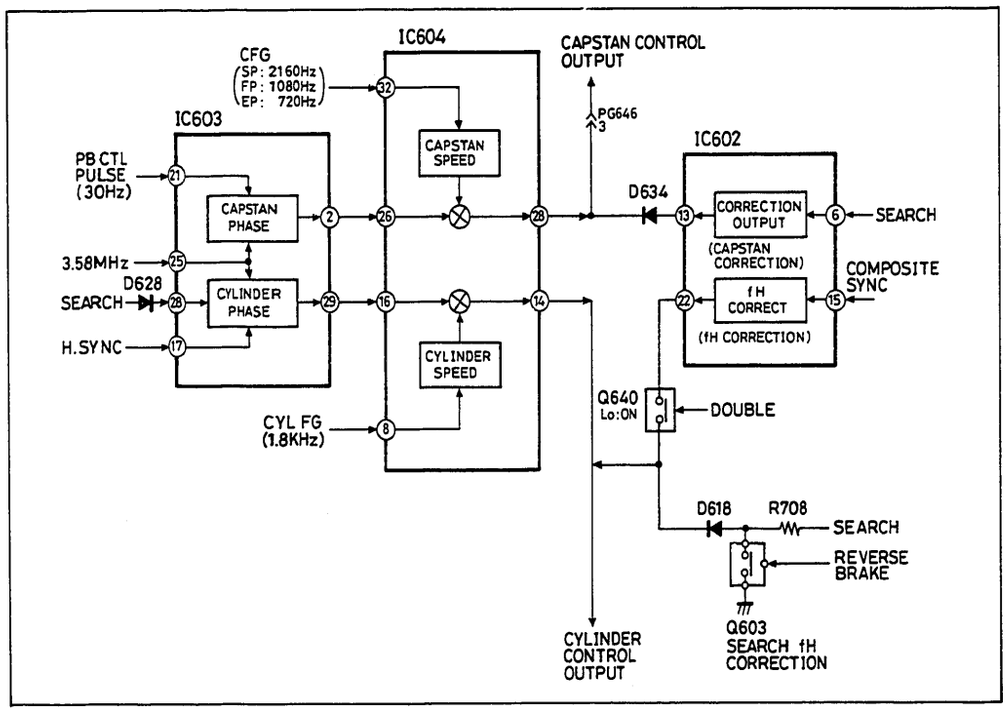



**Fig. 5 Motor Drive Output System in Search**

Trigger signals for search are "SEARCH (Hi)" and "REVERSE (Hi)" supplied to the servo circuit from the μP in the system control circuit. When only the "SEARCH (Hi)" signal is supplied, the forward search mode is entered, and when the "REVERSE (Hi)" is also supplied, the reverse search mode is obtained.
Fig. 5 shows the motor drive system in the search mode. The purpose of the servo circuit in search is to control the capstan motor and cylinder motor, and their operation systems are configured as shown in Table 3.

**Table 3 Control in Search Mode**

| Control System / Motor Controlled | Phase Control | Speed Control | Others |
|---|---|---|---|
| Capstan Motor | Operates | Operates | • Search correction |
| Cylinder Motor | Stops | Operates | • fH correction<br>• Search offset |



### Capstan Motor Control

The capstan motor control outputs are the phase/speed control outputs and the correction output supplied from IC602 pin 13.
The phase control operation is the same as that during normal play and the playback CTL pulse and 3.58 MHz signal are phase compared. The frequency of the CTL pulse gets higher in the search mode, so, to operate the servo system the same as in normal play using this signal, the CTL pulse supplied to IC603 pin 21 is previously divided as follows.

1/5 division in SP
1/9 division in LP
1/15 division in EP

The CTL pulse divided in this way becomes 30 Hz at all tape speeds and is supplied to the phase control system.
Speed control is done by the CFG pulse the same as in normal play. The frequency of the CFG pulse gets higher in the search mode, so, to operate the servo system the same as in normal play using this signal, the CFG pulse supplied to IC604 pin 32 is previously divided as follows.

1/5 division in SP
1/9 division in LP
1/15 division in EP

The CFG pulse divided in this way becomes 2160 Hz in SP, 1080 Hz in LP and 720 Hz in EP, and is supplied to the speed control system.
The correction voltage from IC602 pin 13 is added to the phase/speed control integrated output at IC604 pin 28. This adding operation is required only in the forward search mode; when "SEARCH: Hi" is applied to IC602 pin 6, the voltages preset in the SP, LP and EP modes are output from pin 13.

### Capstan correction output

The tape load increases for the capstan motor in the search mode compared with the normal play mode. At the same time, fH correction is performed for the cylinder motor, so it is required to rotate the capstan motor faster in forward search, and slower in reverse search. The fH correction and tape load have an offset effect in reverse search, but in forward search, fH and the tape load have a multiplication effect. To offset this effect, it is required to add the sufficient correction output only in forward search.

### Cylinder Motor Control

The phase control operation is stopped by the "SEARCH: Hi" signal supplied to pin 28 in the visual search mode, and the PWM wave at pin 29 is set to 50% duty.
The cylinder motor is controlled by the speed control output and fH correction output.
The speed control operation is the same as that in normal play and is performed by the CYL FG pulse (1.8 kHz). This output (IC604 pin 14) is added to the output from the fH correction circuit composed of IC602 and Q603, and the cylinder motor is controlled. Since the relative speed of the tape and cylinder gets higher in forward search in which the tape is fed rapidly in the forward direction, the output from the $f_H$ correction circuit increases the cylinder speed to keep the relative speed normal. Since the relative speed of the tape and cylinder gets lower in reverse search in which the tape is fed rapidly in reverse, so the output decreases the cylinder motor speed to keep the relative speed normal. This control output keeps the frequency of the horizontal sync signal normal in the visual search mode.

### Cylinder output correction

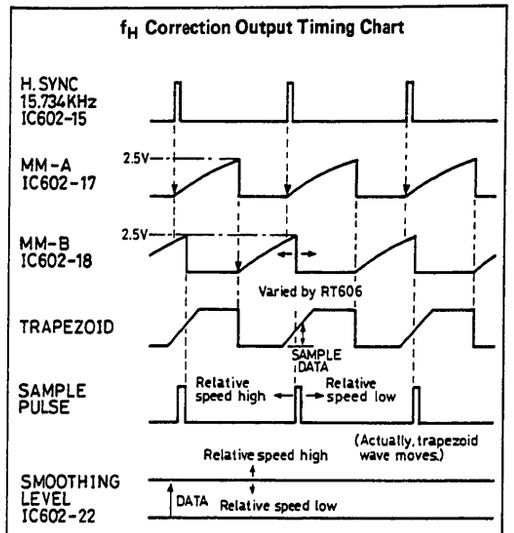
The tape speed becomes faster in visual search compared to normal play, so the relative speed of the cylinder and tape varies causing drift of the horizontal sync frequency ($f_H$) and displacement of luminance/chroma and no color occurs. To prevent these phenomena from occurring, a correction circuit is installed in the cylinder motor output system to correct it ($f_H$ correction). This circuit adds the cylinder acceleration output in forward search in which the relative speed becomes higher, and adds the cylinder deceleration output in reverse search in which the relative speed gets lower.
Previously this $f_H$ correction was done by DC addition (forward search)/output division (reverse search) using a resistance circuit. In this unit, control of sampling the horizontal sync signal is used to improve the correction accuracy.
Fig. 6 shows the cylinder output correction ($f_H$ correction) circuit.
The cylinder output correction circuit in search is positioned around IC602 pins 15 - 22. The output for $f_H$ correction is obtained using this circuit, and it is added or subtracted to/from the cylinder motor control line via pin 22. This output is controlled by the "SEARCH" signal supplied to pin 6 and is effective only during search. The composite sync signal is input via pin 15 to IC602 from the video system and fed to MM-A and the trapezoid generator.
The horizontal sync signal is extracted by MM-A. This extraction operation of the horizontal sync signal is determined by the time constant at pin 17. The horizontal sync signal is fed to MM-B from MM-A.
MM-B determines the rise of the pulse generator in the next stage. As can be seen in the timing chart, when the width of

the pulse in MM-B is varied by RT606 connected to pin 18, the sampling reference position can be moved to the optimum position. The pulse generator in the next stage is triggered by the output of MM-B and generates the pulse used for sampling.

The trapezoid wave and the sampling pulse are compared in the sample hold circuit and the sampling output is generated. This output is converted to DC by the operational amplifier in the next stage. The DC-converted output becomes higher in forward search in which the relative speed is high, and becomes lower in reverse search in which the relative speed is low.

The $f_H$ correction output obtained in IC602 tends to be low in forward search. To compensate this, the "SEARCH: Hi" signal is supplied via R708 to the output of IC602 using Q603 and D618 only in forward search.

In reverse search, Q603 turns on when receiving "REVERSE: Hi" sent from the system control circuit. This is because "SEARCH: Hi" is used only in forward search.



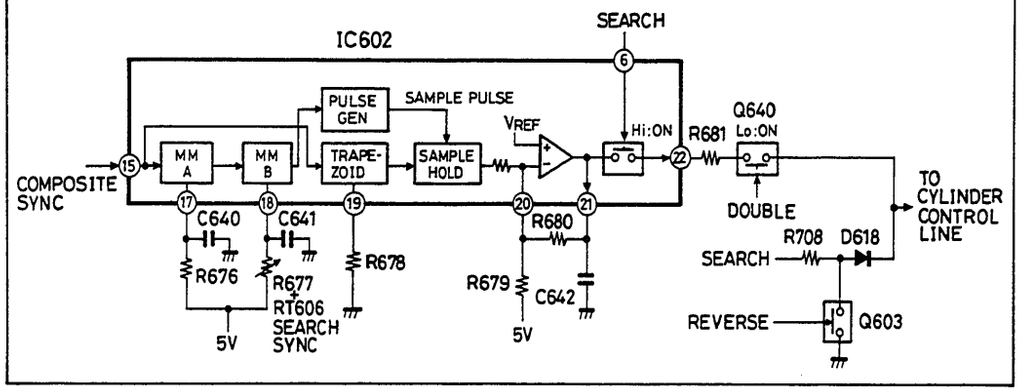
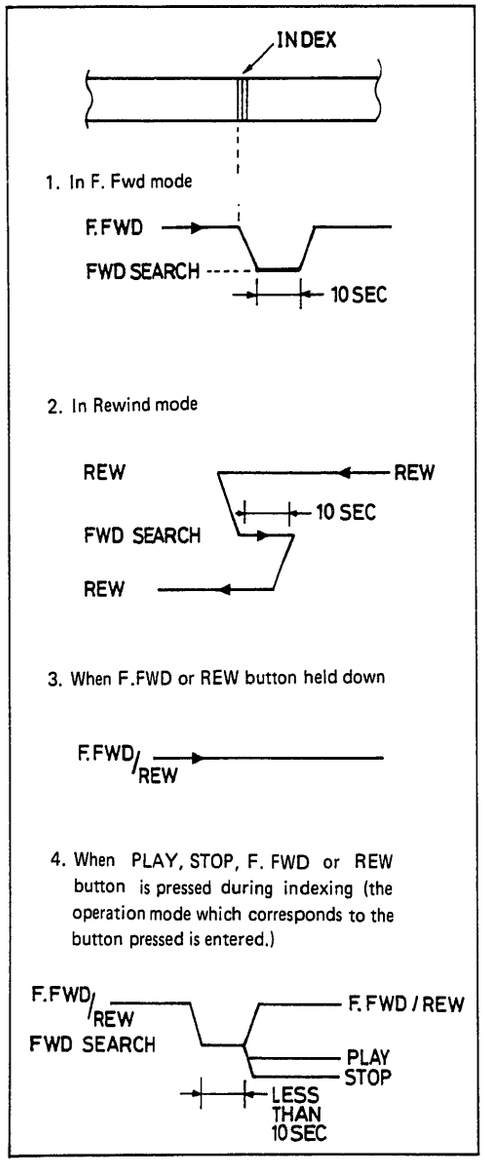




Fig. 6 $f_H$ Correction Circuit

## PROGRAM INDEXING

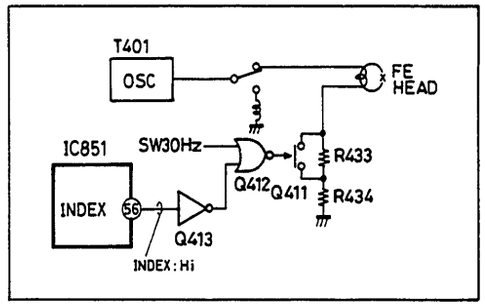
When the fast forward or rewind operation is performed with the Index switch turned on, the unit enters the program indexing operation every time the INDEX signal recorded on the tape is picked up. Program indexing functions so that the unit enters the forward visual search mode for approx. 10 seconds every time the INDEX signal is detected, and then returns to the fast forward or rewind operation again.
When the fast forward, rewind, stop or play is commanded during this search, the search operation is suspended and the unit enters the commanded mode.




**Recording INDEX signal**

- Turn on the Index switch. (Index indicator lights.)
- The erase current modulated by the SW30Hz pulse is automatically recorded as the INDEX signal by the FE head at the start of the recording, timer recording or IRT mode.

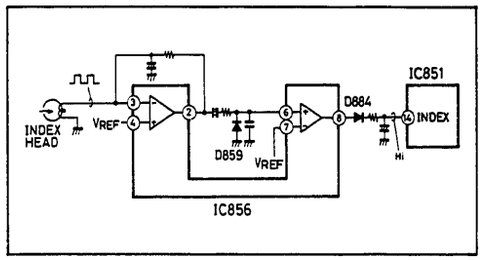
When the programmed times for timer recording overlap, the INDEX signal is automatically recorded at the coupling section.
The INDEX signal is not recorded at the start of recording after the record paused is released.




- When INDEX: Hi is output, Q412 performs binary operation with the SW30Hz signal to drive Q411. The current flowing to the FE head is fluctuated at 30 Hz . . . . . INDEX signal.

**Playing back INDEX signal**

- Turn on the Index switch. (Index indicator lights.)
- When the fast forward or rewind operation is done, the INDEX signal is detected and the interruption of the forward search is performed for only 10 seconds.

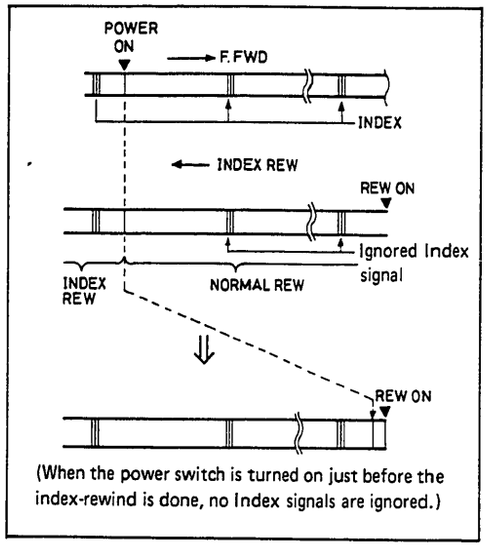



- The 30 Hz component is derived from the signal detected by the index head, and it is amplified and smoothed to obtain the INDEX: Hi signal. This signal is supplied to pin 14 of the system control μP.



**Index-Rewind Correction**

The index-rewind circuit on the system control sub-circuit board performs the following operation for correction of the phenomenon shown below.
Phenomenon: When the tape is advanced by fast forwarding with the power turned on and the index-rewind is performed, the visual search is not done when the INDEX signal is picked up but the tape is simply rewound to the position where the power switch is turned on.
When the tape is rewound and reaches the position where the power is turned on, the normal index-rewind is entered.




(When the power switch is turned on just before the index-rewind is done, no Index signals are ignored.)

Correction: The μPs are reset at the start of the index-rewind to shift the power switch ON position just before the index-rewind starts. Then the index ON and rewind ON operations are performed again.
Doing this, even through the tape advances, the power switch ON position is set just after the index-rewind starts, and the normal index-rewind is performed.

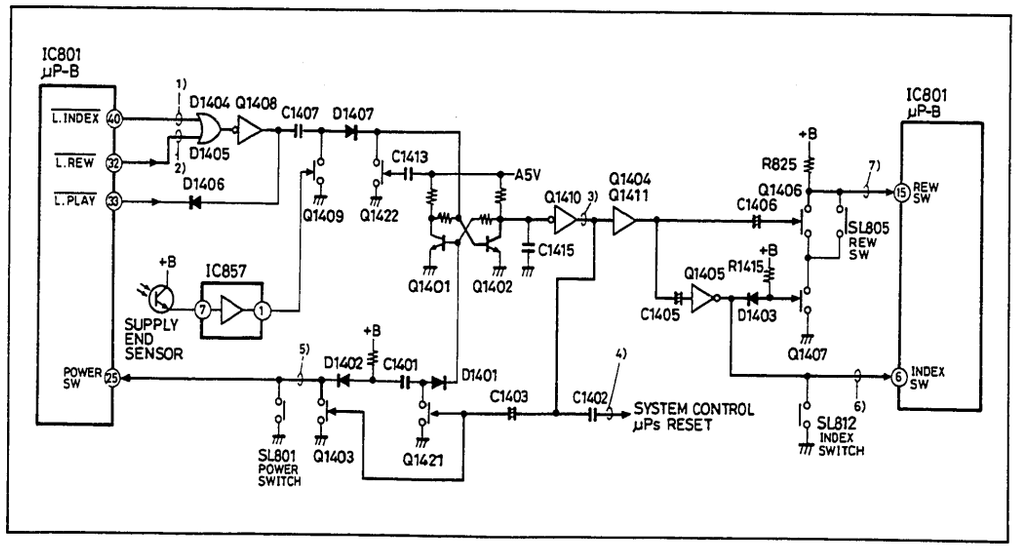
Description of circuit operation:

The figure shows the index-rewind correction circuit. When the Index switch (SL812) is turned on and the μP (IC801) accepts the index mode, IC801 makes pin 40 Lo to light the index indicator. . . . . 1)

When the rewind switch (SL805) operation is accepted by IC801 to perform index-rewind, pin 32 becomes Lo. . . . . 2)

Q1408 is turned off by 1) and 2) and outputs Hi. This output is differentiated by C1407 and is applied to the one-shot multivibrator composed of Q1401/Q1402 and a Hi pulse is obtained through Q1410. The series of operations shown above is performed by this pulse. . . . . 3)

μP reset: A pulse is applied to the reset circuit via C1402 to reset the μP. This sets the power switch OFF. . . . . 4)




**Index-Rewind Correction Circuit**

Power switch ON: The pulse shown in 3) is applied to Q1403 via C1403. Q1403 turns on and has the same effect as power switch ON. The μP is set to the power switch OFF state by the reset pulse. . . . . 5)

Index switch ON: The pulse shown in 3) is applied to Q1405 via C1405. Q1405 turns on and has the same effect as Index switch ON. . . . . 6)

Rewind switch ON: The pulse shown in 3) is applied to Q1406 via C1406. Q1406 turns on and has the same effect as rewind switch ON. Q1407 is connected in series with Q1406, and turns on after the index switch is turned on so the index switch ON has priority over rewind switch ON due to the capacitance difference between C1405 and C1406. Activation of Q1407 sets the rewind switch ON. . . . . 7)

Role of D1406: When the reverse search is performed with the Index switch turned on, the Q1408's output is absorbed by the play indicator output so that it is inhibited and reverse search is not involved in this series of operations.

Role of Q1409: When the auto rewind operation is entered with the Index switch ON, Q1408's output is absorbed by the tape end output so that it is inhibited and auto rewind is not involved in this series of operations.

Role of Q1422: Q1422 initializes the one-shot multivibrator when the power supply is connected.

Role of Q1421: Q1421 sets the one-shot multivibrator to the initial state again after the serial operation is completed.

Q1421 turns off after the serial operation, and a Hi pulse turns on Q1401 via C1401/D1401 to invert the multivibrator.

## COMMUNICATION BETWEEN μPs

### Outline

This unit has μPs with the following functions. Fig. 1 shows the μP communications system. These μPs are provided with the communication buses to exchange data.

- IC851 (System Control μP-A): VTR overall system control, mechanism drive control, switching circuits for each mode. Communicates with IC801 (System Control μP-B) concerning operation mode.
- IC801 (System Control μP-B): Operation mode input and mode indication control.
  Communicates with IC851 (System Control μP-A) and IC1201 (Timer μP) concerning operation modes.
- IC1201 (Timer μP)
  Controls the time count, time and channel number indications on the display.
  IC1201 is positioned between IC801 (System Control μP-B) and IC1701 (Tuning μP). IC1201 transfers the remote mode transmitted from IC1701 to IC801 and the present mode transmitted from IC801 to IC1701.
  IC1201 transfers the channel number, clock set and programs preset for timer recording, which are transmitted from IC1701, and the data concerning the operation mode, transmitted from IC801, to IC52 (Character Generator).
- IC1701 (Tuning μP): Controls channel selection and receives remote control data.
  Communicates with IC1201 (Timer μP) data concerning the remote control. Communicates data with IC1702 (EAROM) concerning channel selection.
- IC51 (Tape Remain μP): Counts the tape counter and tape remaining indication using the pulses sent from the reel disks. The data obtained here is transferred to IC52 (Character Generator).

**1) Communications between System Control μP-B (IC801) and System Control μP-A (IC851)**

System Control μP-A and μP-B perform data transfer via 2 data lines and one clock line.

Fig. 2 shows the System Control μP-A/μP-B data transfer timing chart. Table 1 shows transfer data from μP-A to μP-B. Table 2 shows the transfer data from μP-B to μP-A. The data is composed of 8 bits, and is transferred synchronized with the clock pulse. It requires approx. 1 msec to transfer the 8-bit data, and it is done in 3 msec periods. The data transfer in bit units is done synchronized with the rise of the clock, and the output data from μP-B is transferred by the time difference.

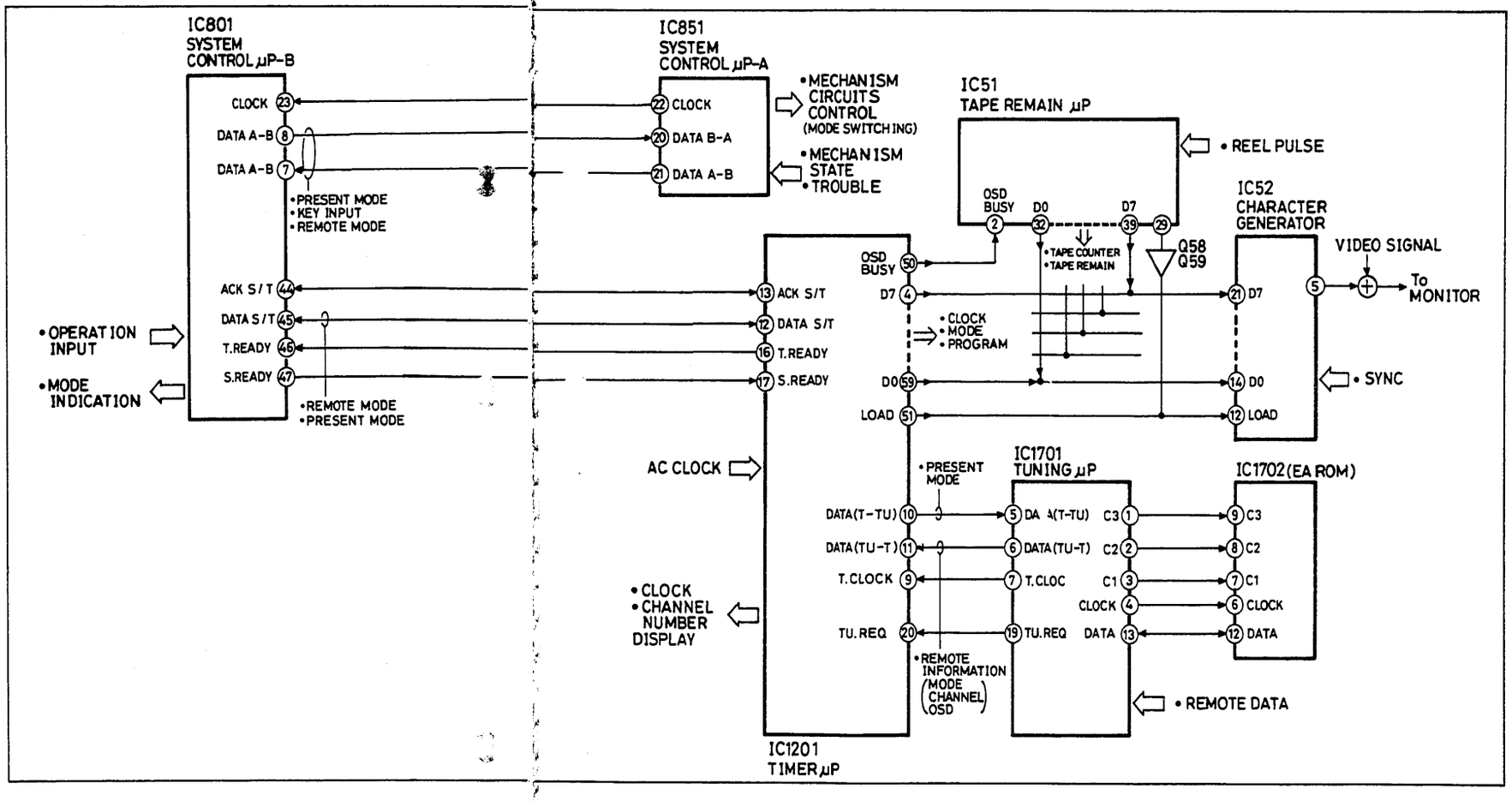



Fig. 1 μP Communications System

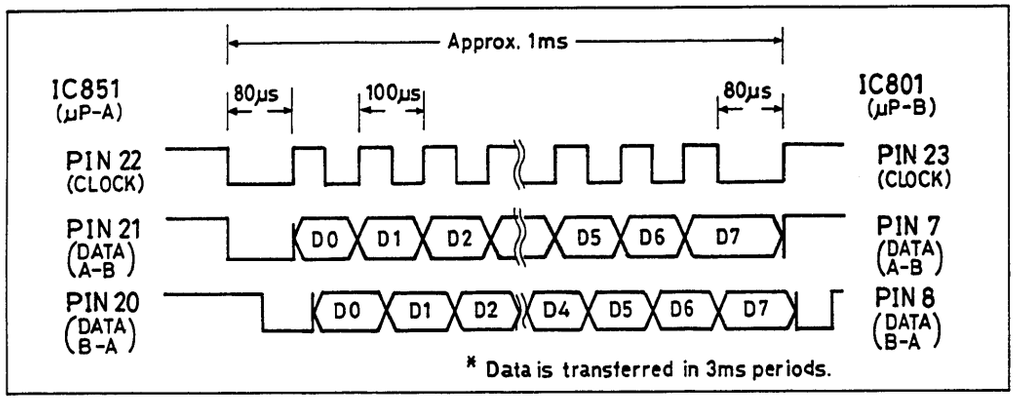



**Fig. 2 System Control μP-A/μP-B Data Transfer Timing Chart**

**Table 1 Transfer Data from μP-A (IC851) to μP-B (IC801)**

*– : 0 or 1 1 : Hi 0 : Lo

| Decimal Notation | Hexadecimal Notation | Binary Notation $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$ | Data |
|---|---|---|---|
| 0 | 0 | – – – 0 0 0 0 0 | CONDENSATION |
| 1 | 1 | – – – 0 0 0 0 1 | PLAY |
| 2 | 2 | – – – 0 0 0 1 0 | RECORD |
| 3 | 3 | – – – 0 0 0 1 1 | A. DUB |
| 4 | 4 | – – – 0 0 1 0 0 | FRAME ADVANCE |
| 5 | 5 | – – – 0 0 1 0 1 | SLOW PLAY |
| 6 | 6 | – – – 0 0 1 1 0 | REVERSE PLAY |
| 7 | 7 | – – – 0 0 1 1 1 | FORWARD SEARCH |
| 8 | 8 | – – – 0 1 0 0 0 | REVERSE SEARCH |
| 9 | 9 | – – – 0 1 0 0 1 | FAST FORWARD |
| 10 | A | – – – 0 1 0 1 0 | REWIND |
| 11 | B | – – – 0 1 0 1 1 | STOP |
| 12 | C | – – – 0 1 1 0 0 | V. DUB |
| 13 | D | – – – 0 1 1 0 1 | — |
| 14 | E | – – – 0 1 1 1 0 | DOUBLE SPEED PLAY |
| 15 | F | – – – 0 1 1 1 1 | — |
| 16 | (1) 0 | – – – 1 0 0 0 0 | EJECT/NO TAPE |
| 17 | (1) 1 | – – – 1 0 0 0 0 | STILL |
| 18 | (1) 2 | – – – 1 0 0 1 0 | RECORD PAUSE |
| 19 | (1) 3 | – – – 1 0 0 1 1 | A. DUB PAUSE |
| 27 | (1) B | – – – 1 1 0 1 1 | STOP PAUSE |
| 28 | (1) C | – – – 1 1 1 0 0 | V. DUB PAUSE |
| | | – 0 0 – – – – – | POWER OFF |
| | | – 0 1 – – – – – | SP |
| | | – 1 0 – – – – – | LP |
| | | – 1 1 – – – – – | EP |
| | | 0 – – – – – – – | INDEX OFF |
| | | 1 – – – – – – – | INDEX ON |

**Table 2 Transfer Data from μP-B (IC801) to μP-A (IC851)**

*1 : Hi 0 : Lo

| Decimal Notation | Hexadecimal Notation | Binary Notation $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$ | Data |
|---|---|---|---|
| 0 | 00 | 0 0 0 0 0 0 0 0 | — |
| 1 | 01 | 0 0 0 0 0 0 0 1 | PLAY |
| 2 | 02 | 0 0 0 0 0 0 1 0 | RECORD |
| 3 | 03 | 0 0 0 0 0 0 1 1 | A. DUB |
| 4 | 04 | 0 0 0 0 0 1 0 0 | FRAME ADVANCE |
| 5 | 05 | 0 0 0 0 0 1 0 1 | SLOW PLAY |
| 6 | 06 | 0 0 0 0 0 1 1 0 | REVERSE PLAY |
| 7 | 07 | 0 0 0 0 0 1 1 1 | FORWARD SEARCH |
| 8 | 08 | 0 0 0 0 1 0 0 0 | REVERSE SEARCH |
| 9 | 09 | 0 0 0 0 1 0 0 1 | FAST FORWARD |
| 10 | 0A | 0 0 0 0 1 0 1 0 | REWIND |
| 11 | 0B | 0 0 0 0 1 0 1 1 | STOP |
| 12 | 0C | 0 0 0 0 1 1 0 0 | V. DUB |
| 13 | 0D | 0 0 0 0 1 1 0 1 | — |
| 14 | 0E | 0 0 0 0 1 1 1 0 | PAUSE |
| 15 | 0F | 0 0 0 0 1 1 1 1 | — |
| 28 | 1C | 0 0 0 1 1 1 0 0 | SLOW SPEED UP |
| 29 | 1D | 0 0 0 1 1 1 0 1 | SLOW SPEED DOWN |
| 35 | 23 | 0 0 1 0 0 0 1 1 | EJECT |
| 45 | 2D | 0 0 1 0 1 1 0 1 | POWER ON |
| 46 | 2E | 0 0 1 0 1 1 1 0 | POWER SWITCH ON/OFF |
| 47 | 2F | 0 0 1 0 1 1 1 1 | POWER OFF |
| | 30 | 0 0 1 1 0 0 0 0 | INDEX ON/OFF |
| | 3C | 0 0 1 1 1 1 0 0 | DOUBLE SPEED PLAY |



**2) Communications between Timer μP (IC1201) and System Control μP (IC801)**

Timer μP and System Control μP perform "shakehands" data transfer via 4 lines - one data line, 2 READY lines which inform the reception μP that the transmission μP is standing by for data transmission and one "$\overline{\text{ACK S/T}}$" line which informs the transmission μP that the reception μP is standing by for data reception.

Fig. 3 shows the data transfer timing chart from Timer μP to System Control μP-B. When data is transferred to Timer μP from System Control μP, "S. READY" is used in place of "T. READY". Table 3 shows the transfer data (first word) from Timer μP to System Control μP-B.

Table 4 shows the transfer data (first word) from System Control μP-B to Timer μP. Data is transmitted every time "READY" rises, and is received every time "ACK S/T" rises. In this "handshakes" data transfer, the data transferred at one time consists of 2 words; the first word is transferred, then the inverted word is transferred as the second word. Data is composed of 16 bits. The transmission/reception operation is repeated 16 times in one data transfer.

Data is transmitted and received through the following steps;

| <Process> | <Transmission μP> | <Reception μP> |
|---|---|---|
| Step 1 | Transmits "READY" → | Receives "READY" |
| | ↓ * | |
| Step 2 | Receives "ACK" ← | Transmits "ACK" |
| | ↓ | ↓ * |
| Step 3 | Stops transmitting "READY" Transmits data → | Stops transmitting "ACK" Receives data |

The following is data transfer when Timer μP transmits data and System Control μP-B receives data.

| (Timer μP (IC1201)) | (System Control μP-B (IC801)) |
|---|---|
| Sets pin 16 "T. READY" to Lo to inform that the μP is standing by for transmission. → | Pin 46 "T. READY" becomes Lo and the μP detects transmission standby. ↓ |
| Judges that the μP-B can receive data when pin 13 "$\overline{\text{ACK S/T}}$" becomes Lo. ← | Sets pin 44 "$\overline{\text{ACK S/T}}$" to Lo when the μP is standing by for reception. |
| Sets pin 16 "T. READY" to Hi. Transmits the 1st word MSB "$\overline{\text{D7}}$" at the rise of this signal. → | Sets pin 44 "$\overline{\text{ACK S/T}}$" to Hi. Reads the transmitted data at the rise of this signal. |

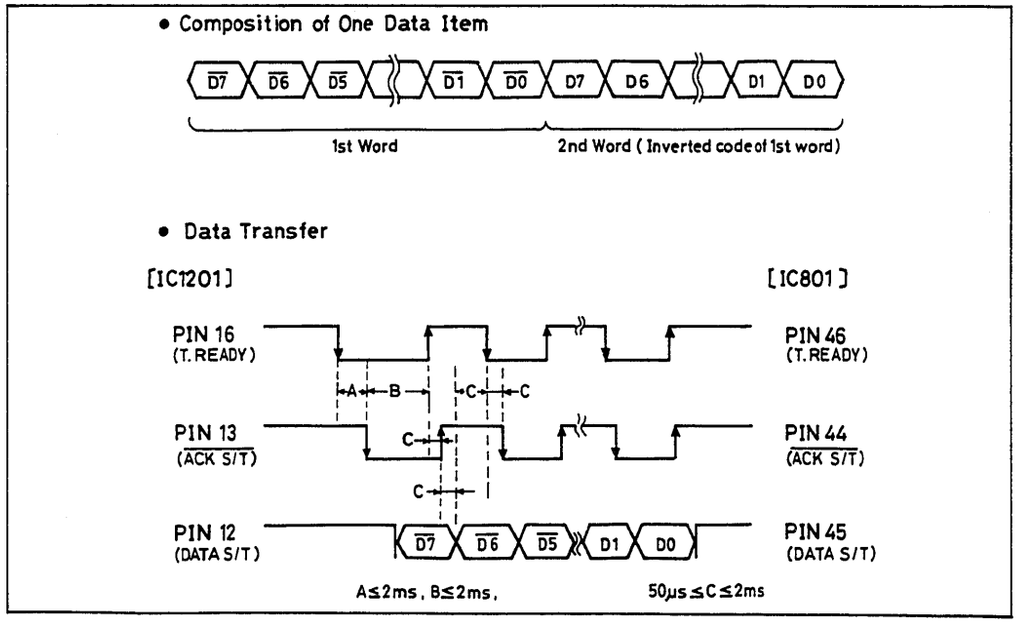



**Fig. 3 Timer μP/System Control μP-B Data Transfer Timing Chart**

The process shown above is repeated up to the 1st word "$\overline{D0}$", and then 2nd word "D7" to "D0" are transmitted in sequence and transmission/reception is completed.

**Table 3 Transfer Data from Timer μP (IC1201) to System Control μP-B (IC801)**

*– : 0 or 1  1 : Lo  0 : Hi

The transfer data is 16 bits; the 1st word and then the 2nd word (1st word) are transmitted.

| Decimal Notation | Hexadecimal Notation | Binary Notation $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | Data (1st Word) |
|---|---|---|---|
| 0 | 00 | 0 0 0 0 0 0 0 0 | BUTTON RELEASE |
| 1 | 01 | 0 0 0 0 0 0 0 1 | PLAY |
| 2 | 02 | 0 0 0 0 0 0 1 0 | RECORD |
| 3 | 03 | 0 0 0 0 0 0 1 1 | A. DUB |
| 4 | 04 | 0 0 0 0 0 1 0 0 | FRAME ADVANCE |
| 5 | 05 | 0 0 0 0 0 1 0 1 | SLOW PLAY |
| 6 | 06 | 0 0 0 0 0 1 1 0 | REVERSE PLAY |
| 7 | 07 | 0 0 0 0 0 1 1 1 | FORWARD SEARCH |
| 8 | 08 | 0 0 0 0 1 0 0 0 | REVERSE SEARCH |
| 9 | 09 | 0 0 0 0 1 0 0 1 | FAST FORWARD |
| 10 | 0A | 0 0 0 0 1 0 1 0 | REWIND |
| 11 | 0B | 0 0 0 0 1 0 1 1 | STOP |
| 12 | 0C | 0 0 0 0 1 1 0 0 | V. DUB |
| 13 | 0D | 0 0 0 0 1 1 0 1 | —— |
| 14 | 0E | 0 0 0 0 1 1 1 0 | PAUSE |
| 15 | 0F | 0 0 0 0 1 1 1 1 | —— |
| 28 | 1C | 0 0 0 1 1 1 0 0 | SLOW SPEED UP |
| 29 | 1D | 0 0 0 1 1 1 0 1 | SLOW SPEED DOWN |
| 30 | 1E | 0 0 0 1 1 1 1 0 | REPEATED TRANSMISSION REQUEST |
| 34 | 22 | 0 0 1 0 0 0 1 0 | EJECT |
| 44 | 2C | 0 0 1 0 1 1 0 0 | POWER ON |
| 45 | 2D | 0 0 1 0 1 1 0 1 | POWER SWITCH OPERATION |
| 46 | 2E | 0 0 1 0 1 1 1 0 | POWER OFF |
| 76 | 3C | 0 0 1 1 1 1 0 0 | DOUBLE SPEED PLAY |

**Table 4 Transfer Data from System Control μP-B (IC801) to Timer μP (IC1201)**

*– : 0 or 1  1 : Lo  0 : Hi

The transfer data is 16 bits; the 1st word and then 2nd word (1st word) are transmitted.

| Decimal Notation | Hexadecimal Notation | Binary Notation $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | Data (1st Word) |
|---|---|---|---|
| 0 | 00 | 0 0 0 0 0 0 0 0 | CONDENSATION |
| 1 | 01 | 0 0 0 0 0 0 0 1 | PLAY |
| 2 | 02 | 0 0 0 0 0 0 1 0 | RECORD |
| 3 | 03 | 0 0 0 0 0 0 1 1 | A. DUB |
| 4 | 04 | 0 0 0 0 0 1 0 0 | FRAME ADVANCE |
| 5 | 05 | 0 0 0 0 0 1 0 1 | SLOW PLAY |
| 6 | 06 | 0 0 0 0 0 1 1 0 | REVERSE PLAY |
| 7 | 07 | 0 0 0 0 0 1 1 1 | FORWARD SEARCH |
| 8 | 08 | 0 0 0 0 1 0 0 0 | REVERSE SEARCH |
| 9 | 09 | 0 0 0 0 1 0 0 1 | FAST FORWARD |
| 10 | 0A | 0 0 0 0 1 0 1 0 | REWIND |
| 11 | 0B | 0 0 0 0 1 0 1 1 | STOP |
| 12 | 0C | 0 0 0 0 1 1 0 0 | V. DUB |
| 13 | 0D | 0 0 0 0 1 1 0 1 | —— |
| 14 | 0E | 0 0 0 0 1 1 1 0 | DOUBLE SPEED PLAY |
| 15 | 0F | 0 0 0 0 1 1 1 1 | —— |
| 16 | 10 | 0 0 0 1 0 0 0 0 | EJECT |
| 17 | 11 | 0 0 0 1 0 0 0 1 | STILL |
| 18 | 12 | 0 0 0 1 0 0 1 0 | RECORD PAUSE |
| 19 | 13 | 0 0 0 1 0 0 1 1 | A. DUB PAUSE |
| 27 | 1B | 0 0 0 1 1 0 1 1 | STOP PAUSE |
| 28 | 1C | 0 0 0 1 1 1 0 0 | V. DUB PAUSE |
| 30 | 1E | 0 0 0 1 1 1 1 0 | REPEATED TRANSMISSION REQUEST |

### 3) Communications between Tuning μP (IC1703) and Timer μP (IC1201)

Tuning μP and Timer μP perform "shakehands" data transfer via 4 communication lines composed of 2 data transfer lines and "REQUEST" line and "T. CLOCK" line. Fig. 4 shows the data transfer timing chart between Timer μP and Tuning μP. Table 5 shows the transfer data code from Tuning μP to Timer μP and Table 6 shows the transfer data code from Timer μP to Tuning μP. The two μPs perform data transfer in 8-bit units while the "REQUEST" pins are Lo.

The following data is transferred from Tuning μP to Timer μP.

- In the channel data, the 10's digit is the higher 4 bits, and the 1's digit is the lower 4 bits, and 0 ~ 9 with the higher 4 bits and 0 ~ 9 with the lower 4 bits are used to indicate 99 channels.
- In the data concerning the mode designation and position designation from the remote control unit, the higher 4 bits are shown as codes A and B.
- In the code concerning the AFT and band, the higher 4 bits are shown as 0 ~ 2, and lower 4 bits as C ~ F.

The following data is transferred from Timer μP to Tuning μP:

- In the channel data, 10's digit is the higher 4 bits, and the 1's digit is the lower 4 digits. 99 channels are shown using 0 ~ 9 as the higher 4 digits and 0 ~ 9 as the lower 4 digits.
- In the code concerning the channel up/down and preset enable/disable by operating the VTR, the higher 4 bits is shown as D, and the lower 4 bits, as 2, 3, 7 or 8.

Data is transferred from Timer μP to Tuning μP as follows.

Timer μP  Tuning μP

a. Sets pin 20 to Lo from Hi. → b. Sets pin 7 to Lo from Hi.

[Communicates that Timer μP is standing by for data transmission]

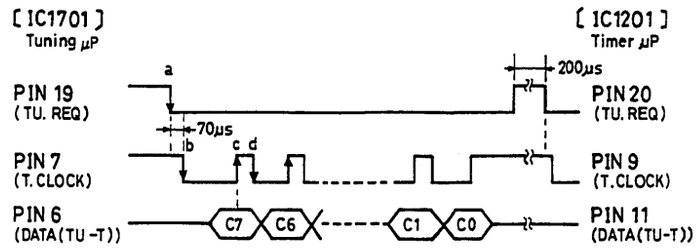
[Communicates that Tuning μP is standing by for data reception]

Sets the "C7" data to pin 10 for transmission. → c. Reads the "C7" data at the rise of Pin 7.

d. Sets pin 9 to Lo from Hi, and complete transmission.

One data transfer is completed by repeating processes "c" and "d" 8 cycles. Data transfer from Tuning μP to Timer μP is performed in the same way.

[ Tuning μP→Timer μP Data Transfer Timing Chart ]




[ Timer μP→Tuning μP Data Transfer Timing Chart ]

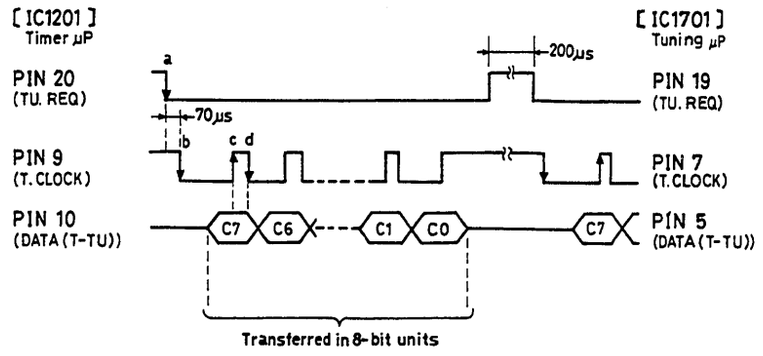



**Fig. 4 Timer μP/Tuning μP Data Transfer Timing Chart**

**Table 5 Codes in Data transferred from Tuning μP (IC1701) to Timer μP (IC1201)**

| Higher 4-Bit (D7 – D4) Codes \ Lower 4-Bit (D3 – D0) Codes | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | NO OPERATION | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | – | – | | SELECT OFF | – | – |
| 1 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | – | – | VHF-L | VHF-L | (CATV) | UHF |
| 2 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | – | – | – | – | AFT ON | AFT OFF |
| 3 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | – | – | – | – | – | – |
| 4 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | – | – | – | – | – | – |
| 5 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | – | – | – | – | – | – |
| 6 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | – | – | – | – | – | – |
| 7 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | – | – | – | – | – | – |
| 8 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | – | – | – | – | – | – |
| 9 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | – | – | – | – | – | – |
| A | SLOW TRACK UP | SLOW TRACK DOWN | SLOW SPEED UP | SPEED DOWN | 8 | 9 | – | – | REV SEARCH | F. FWD | REW | STOP | 0 | 1 | 2 | 3 |
| B | F. ADV | SLOW PLAY | DOUBLE SPEED | FWD SEARCH | PLAY | – | VTR | POWER SW | CH UP | CH DOWN | STILL /PAUSE | REV PLAY | 4 | 5 | 6 | 7 |
| C | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – |
| E | – | KEY "BUTTON" RELEASE | – | – | – | – | – | – | – | – | – | – | – | – | – | – |

**Table 6 Codes in Data transferred from Timer μP (IC1201) to Tuning μP (IC1701)**

| Higher 4-Bit (D7 – D4) Codes \ Lower 4-Bit (D3 – D0) Codes | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | NO OPERATION | 01 CH | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | – | – | – | – | – | – |
| 1 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | – | – | – | – | – | – |
| 2 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | – | – | – | – | – | – |
| 3 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | – | – | – | – | – | – |
| 4 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | – | – | – | – | – | – |
| 5 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | – | – | – | – | – | – |
| 6 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | – | – | – | – | – | – |
| 7 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | – | – | – | – | – | – |
| 8 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | – | – | – | – | – | – |
| 9 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 | – | – | – | – | – | – |
| A | SLOW TRACK UP | SLOW TRACK DOWN | – | – | 8 | 9 | – | – | – | – | – | – | 0 | 1 | 2 | 3 |
| B | – | – | – | – | – | – | – | – | – | – | – | – | 4 | 5 | 6 | 7 |
| D | – | – | CH UP | CH DOWN | – | – | – | PRESET DISABLE | PRESET ENABLE | – | – | – | – | – | – | – |



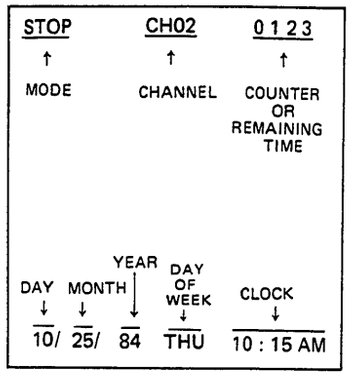
## ON SCREEN DISPLAY (OSD) Function

This unit uses the OSD function and the following informations can be monitored on the screen.

The following are the OSD information and display area.

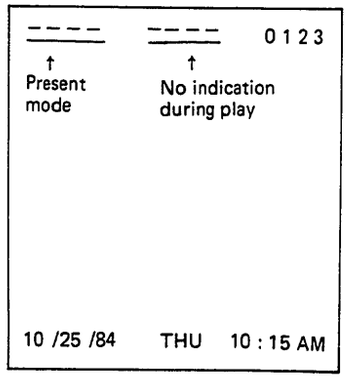
- VTR modes (Stop, Record, etc.)
- Channel number
- Tape counter or tape remaining time
- Month/day/year/day of week
- Time

Time setting and program setting (1-year/8-program) other than the above are performed using the OSD.

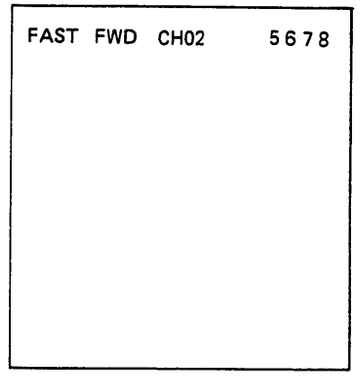



**Indications are given in the following cases.**

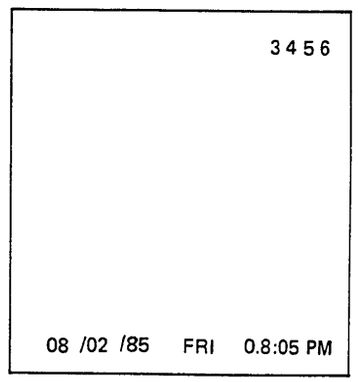
1) For 20 seconds after the power switch is turned on or for 5 seconds after the DISPLAY button on the remote control unit is pressed.
   When the power switch is operated, the same information as the above is displayed. When the DISPLAY button is operated, the present mode in which the VTR is placed is displayed. When the present mode is PLAY, the channel number is not displayed.




2) For 5 seconds after the mode is changed.
   The following are the modes which are displayed after being changed.
   The object information at this time is the mode/channel number/counter or tape remaining time.
   - PLAY (No channel indication)
   - RECORD
   - RECORD PAUSE (Indicated as "PAUSE")
   - STOP
   - FAST FORWARD
   - REWIND




3) When the DISPLAY button on the remote control unit is pressed in the state shown in 1), only the counter or tape remaining time is displayed.
   The counter or tape remaining time can be selected by the COUNTER and TIME REMAIN buttons on the front panel of the VTR.
4) When the DISPLAY button on the remote control unit is pressed in other modes (search, still, etc.) than the modes shown in 2), the mode and the channel number are not displayed.

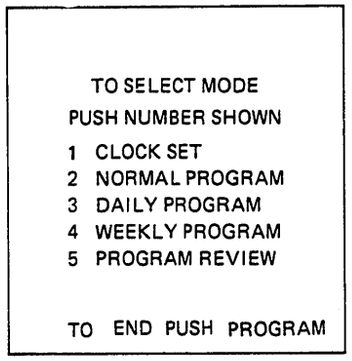


**Time setting and program setting**

Time and programs are set using the OSD in this unit. They are set by operating the buttons on the remote control unit according to the instructions appearing on the screen.

**[How to set]**

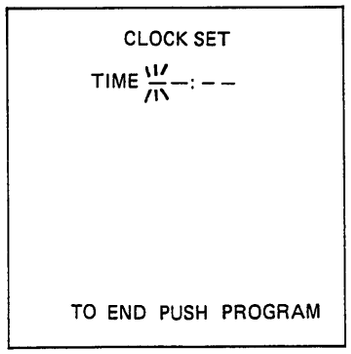
1. Turn on the power switch.
2. Press the PROGRAM button in the stop, record or record pause mode.
3. The background of the screen becomes black and the program menu appears. This indication continues for 1 minute. When there is no input for this time, the indication is cleared.



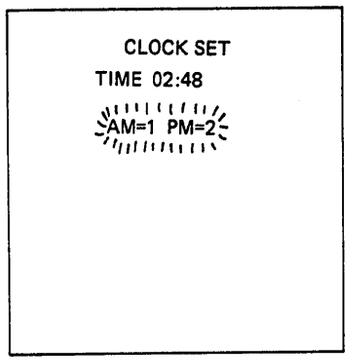

4. Select the object to be set using buttons 1 ~ 5. The VTR enters the sequence for programing information for the selected program No.

**[Time setting]**

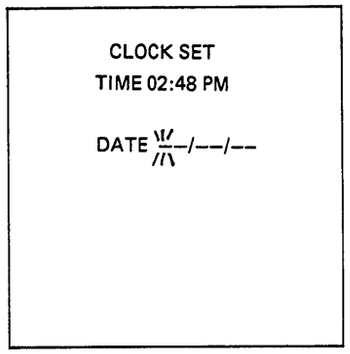
1. Select "1" in the program menu.
   The OSD enters the time setting sequence.
2. The first bar (left end) flashes in the time display. For an example, set PM 2:48, Friday, August 24, '84 as follows.



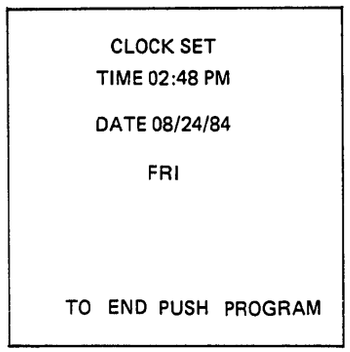

3. Set the time "02:48".
   Simultaneously when the time is set, the AM/PM selection sequence "AM:1, PM:2" flashes.




4. Set PM to "2".
   Simultaneously when "2" (PM) is set, the date input sequence is entered.




5. Set the date "08/24/84".
   The day of the week is automatically determined.



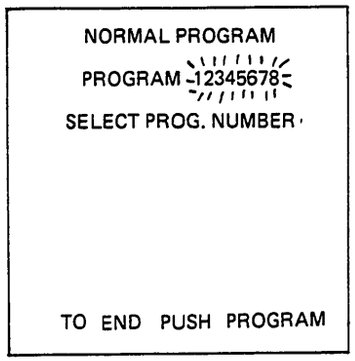

6. Correct the inputs to clear each digit using the "CLEAR" button and input the correct informations again.
7. Press the PROGRAM button to finish setting.
   Seconds start counting when the PROGRAM button is pressed. When the PROGRAM button is not pressed for more than 1 minute after the final character is set, the indication on the screen returns to its original state and time setting becomes invalid.



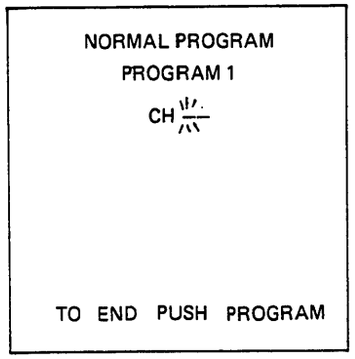
**[Normal program setting]**

The longest programmable time is 23 hours 59 minutes. When the start time (ON) and stop time (OFF) match, the program setting is accepted but it is cleared automatically by the $\mu$P.

1. Select "2" in the program menu.
   The OSD enters the normal program setting sequence.
2. The program Nos. having no informations flash. For example, program "Program No. 1, 1984, Jan. 29, 1:23 PM ~ 4:56 PM, 7CH" as follows, assuming today to be Jan. 28, '84.

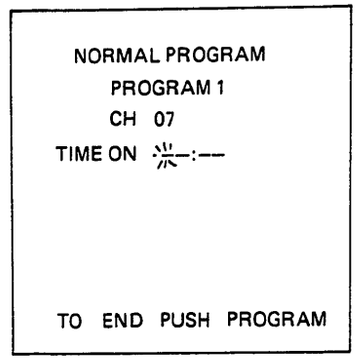



3. Set program number 1.
   The channel setting sequence is entered simultaneously when program number 1 is set.
   The 10's digit bar the channel number flashes.

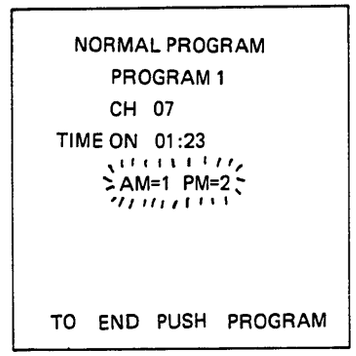



4. Set channel number "07".
   (When "0" is set, the 1's digit bar flashes, so set "7" in sequence.)
   When the channel number is determined, the recording start time setting sequence is entered. The 10's hour digit bar flashes.

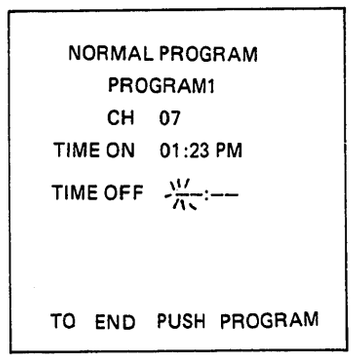





5. Set the time by operating "01:23".
   When the start time is determined, the AM/PM selection sequence is entered.

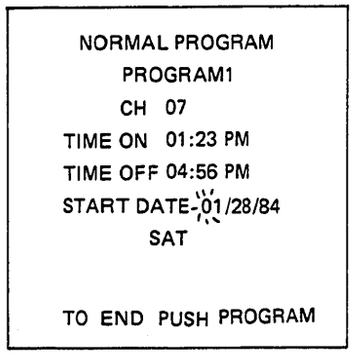



6. Select "PM" by operating "2".
   When "PM" is determined, the recording stop time setting sequence is entered. The 10's hour digit bar flashes.

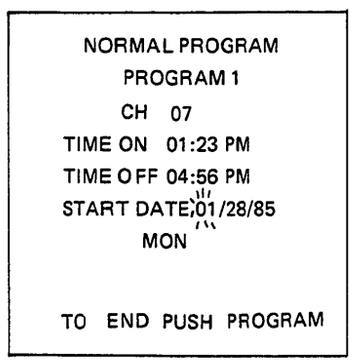


7. Set the stop time in the same way as setting the start time.
   Input "56 minutes after 4 PM" by operating "04:56 2".
   The recording date programming sequence is entered.
   "Today" is indicated as the programmed day.
   Note: As for the programmed date, when the stop (OFF) time is in the past, today in the next year is displayed as "Jan. 28, '85".
   The 10's digit of the programmed month flashes.

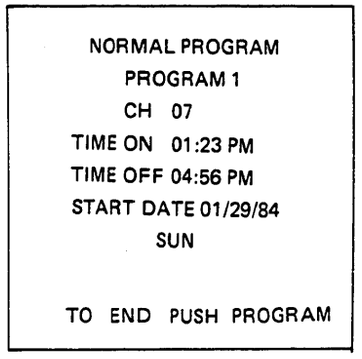
**[The OFF time is in the future from the present time]**




**[The OFF time is in the past from the present time]**




8. When "01/29" is input, '84 (this year) SUN" is automatically calculated and displayed.
   However, when this "01/29" is a month and day before today, "01/29" is automatically judged in the next year and "85 (1985: next year) TUE" is displayed.




9. Press the PROGRAM button to finish programming.
   The input correction operation is the same as for time setting.
   When an illogical input is done, for example, when 2 or more numerals are input as the 10's hour digit, the "?" indicator flashes.

**[Daily program setting]**
The procedure is the same as that in normal program setting except that "DAILY PROGRAM" is displayed on the OSD.
Recording is made on the days of the week excluding Saturday and Sunday.
However, if the start day is Saturday or Sunday, recording is made on Saturday or Sunday only for that week, and from the next week recordings are made only on the usual weekdays.

**[Weekly program setting]**
The procedure is the same as that in normal program setting except that "WEEKLY PROGRAM" is displayed on the OSD.

**[Program review and cancel]**
Select "5" in the program menu to review the programmed information. The OSD displays the preset programs for 10 seconds each. When the "5" button is pressed during display, the next programmed contents are displayed. To cancel a program, press the "CLEAR" button while reviewing the information of the program.

## VIDEO CIRCUIT

The basic operation and composition of the video circuit are almost the same as those in a conventional VTR.
Since the VT-89A features the OSD function, the circuits mainly composed of the following ICs are newly added to the conventional VTR.
Schematic operations of all ICs are described in the following, and the new circuits Nos. are noted in bold characters.

IC201: Playback preamplifier, Playback AGC, Record emphasis, FM Record Y/C MIX.

IC202: FM demodulator, Deemphasis, Play Y/C mixer, Record AGC, Sync separation.

IC203: Play/record chroma process.
IC204: Video head record/play/field play switching.
IC205: Edge noise cancel.
Suppresses the edge noise generated at the rise and fall of the video signal in the EP mode.

IC206: 1H correlative noise cancel.
Demodulates the FM signal delayed by 1H using the different system (IC206), extracts random noise by use of the difference with the main signal (signal demodulated by IC202) and adds it again with its phase in reverse to the main signal to reduce random noise in the main signal.

IC207: Play equalizer, switch of peaking characteristics in trick play, switch of EP dynamic emphasis characteristics.

**IC208:** Record signal selection.
Transmits the video signal to the record system when it is present, and when the video signal is not present (only Hi-Fi audio is recorded), transmits the sync signal generated in the different system (IC212: sync Signal Generator) to the record system to record it.

**IC209:** Play picture control.
The video signal does not pass through the picture control amp during recording but passes through it only during play.

**IC210:** Play/EE video signal output selection.
Selects the sync signal generated by IC212 and makes the monitor screen black in the OSD mode or when there is no video signal (when playing a blank tape).

**IC211:** Sync signal detector.
Detects the presence/absence of the sync signal in the record video signal, and the sync signal in the playback video signal. Performs switching of the sync signal route by the detection signal.

**IC212:** Sync signal generation
Generates the sync signal for use when recording or playing back no signal. The reference signal for the TV screen synchronization and when playing a tape without a video signal

**Video System Recording Operation**

Fig. 1 shows the video signal recording circuit.
The composition is basically the same as that in other VTRs as seen from the figure, so only operations concerning IC208, IC211, and IC212 are described in the following.
IC208 receives the record video signal via pin 7 and the sync signal sent from sync generator (IC212) via pin 2. These signals are switched by the level at pin 3 and output at pin 4, then sent to the FM circuit, video heads in sequence. Pin 3 becomes Hi due to the output from pin 9 of the sync detector (IC211) when receiving no video signal and the sync signal from pin 2 is output at pin 4. That is, only the sync signal is recorded on the video track when recording only the audio signal. **This makes the screen completely black, and noise is no problem when the tape remaining time or counter is displayed and only numerals are indicated.**
In the record mode without video, the servo circuit operates the same as in the normal record mode because of the sync signal sent from the sync generator (IC212).

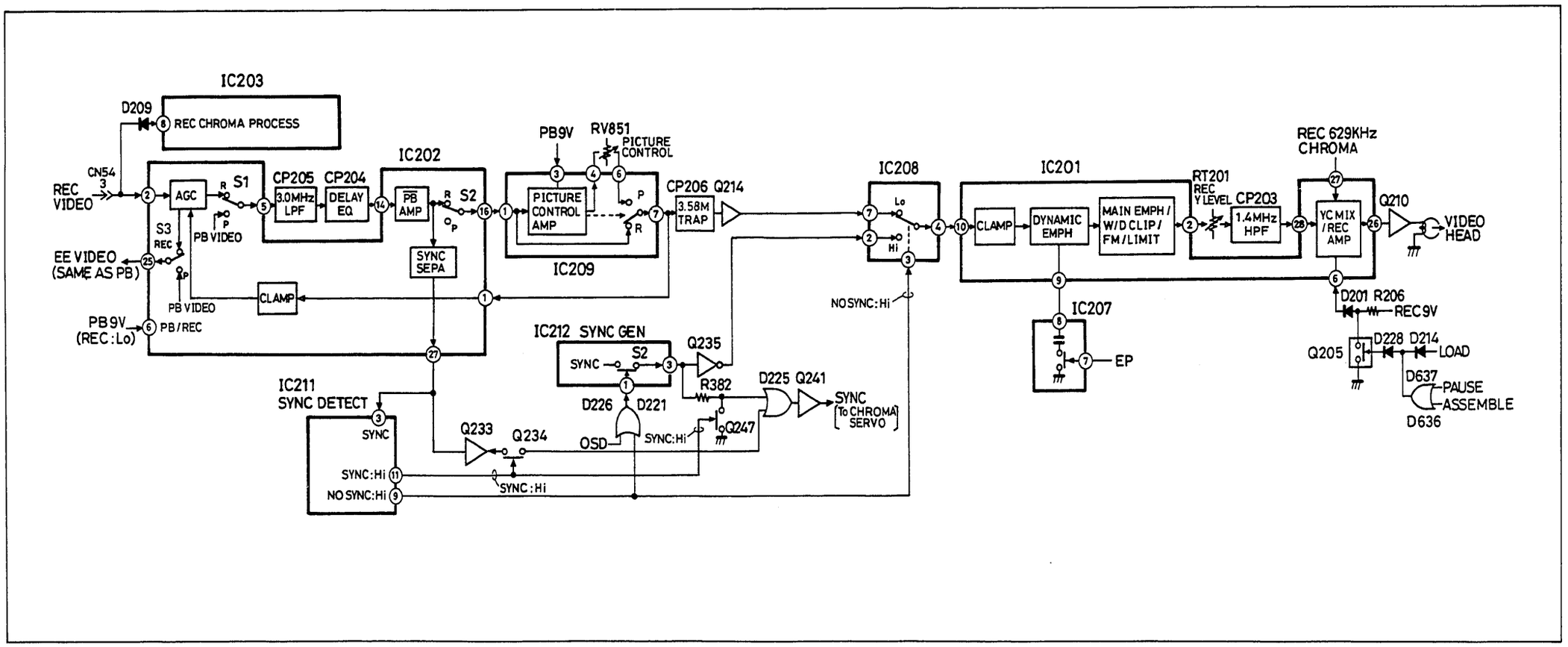



Fig. 1 Video Signal Recording Process

### Sync Detector (IC211), Sync Generator (IC212)

Fig. 2 shows the sync detector and the sync generator. These detect the presence/absence of the composite sync signal obtained by the sync separator in the video processing system (IC202). When recording the audio signal in models equipped with VHS Hi-Fi (when the unit is used as an audio deck), the reference signal which controls the cylinder motor is not present, so it is required to generate an artificial sync signal. The sync signal in the video signal is previously detected by IC211, and when there is no sync signal, the artificial sync signal is generated by IC212.
IC211 sets pin 11 to Hi when it detects the sync signal, and sets pin 9 to Hi when it does not detect the sync signal. IC212 generates the artificial sync signal via pin 3 when pin 1 is Hi.

### IC211 Operation

IC211 receives the output from the sync separator in IC202 via pin 3. IC211 removes th H.sync component from this output using the LPF and smoothes it through the smoother. When the V.sync component is present, inverter-1 outputs Lo and inverter-2 outputs Hi. On the other hand, when there is no V.sync component, inverter-1 outputs Hi.

IC211 receives the vertical drive pulse generated in the servo circuit via pin 2, and the vertical drive pulse is smoothed in place of the V.sync component even when a tape is played back in the mode in which the sync signal is distorted during trick play. This vertical drive pulse line is connected only during play when the PB 9V signal is output.

### IC212 Operation

IC212 pin 6 receives the 3.58 MHz chroma sub-carrier signal sent from IC203 pin 16. This signal is divided into 114 in IC212. The 1/114-divided output is fed to the 1/525 divider via S1. S1 is the PAL/NTSC switch which is changed by the level at pin 8; it sets pin 8 to Lo in the NTSC mode and uses the 1/525 divider. The 60Hz signal obtained here is decoded by the decoder to form the artificial sync signal shown in the figure. The artificial sync signal is output at pin 3 via S2. S2 is controlled by the level at pin 1. The "NO SYNC (pin 9)" signal from IC211 and the "OSD" signal sent from the character generator (IC52) are applied to pin 1, and the artificial sync signal is output at pin 3 when recording and playing back no signal as well as in the OSD mode.

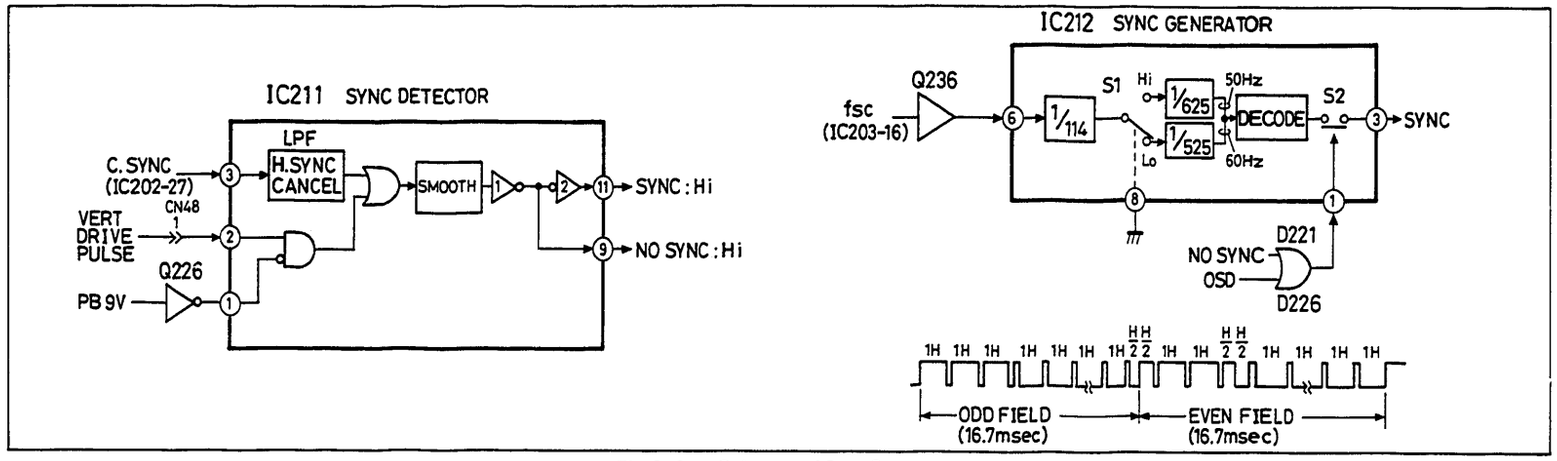



Fig. 2 Sync Delector and Sync Generator

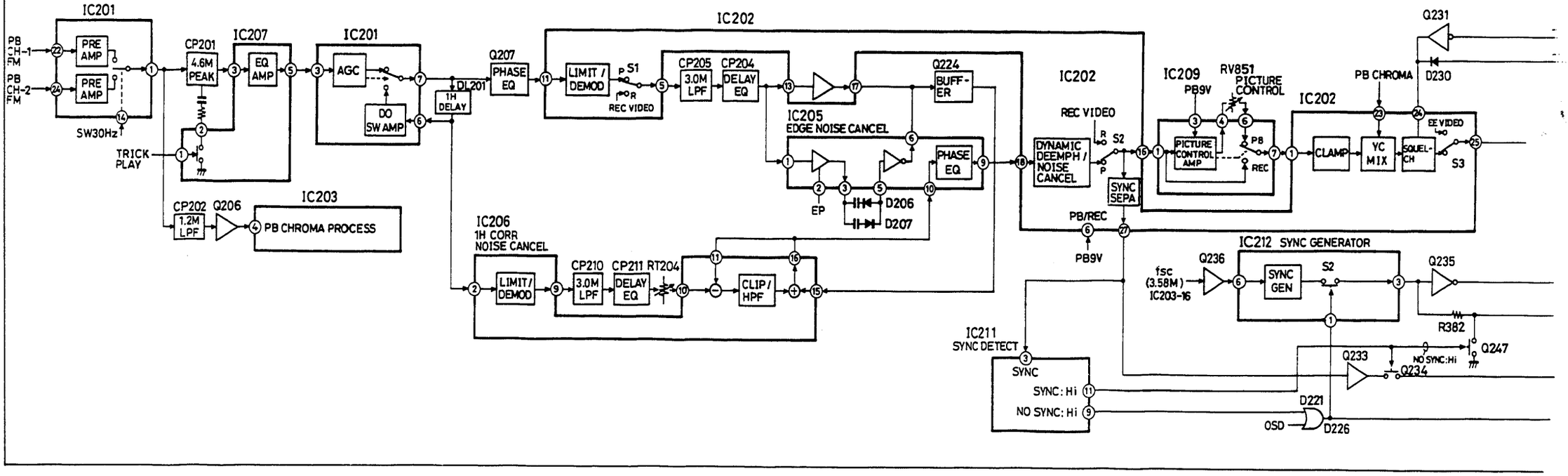



Fig. 3 Video Signal Playback Process

### Video System Playback Operation

Fig. 3 shows the video signal playback circuit.
As can be seen from the figure, the basic operations of the playback system are the same as for a conventional VTR. Operations concerning IC210 are described in the following. IC210 receives the sync signal sent from the sync generator (IC212) via pin 2, and the playback video signal via pin 7. Pin 3 is supplied with the output (set to Hi when no sync signal is present) at pin 9 of the sync detector (IC211) and the "OSD" mode signal.
In the OSD mode or when playing a tape on which only the audio signal is recorded by a VTR having no sync signal recording function, the sync signal is output as a video output.* With this output, the character generator also operates in the cases shown above.
When the OSD is used or when the tape remaining time and counter indications are done, the OSD character signals are added to the video output system by Q232 from the character generator (IC52). The brightness of the characters at this time is lowered by Q244 and R373.

* When playing a blank tape, the white noise component in the playback signal contains a component similar to the sync signal, so the sync detector, in many cases, judges that the sync signal is present.

### Video System EE Operation

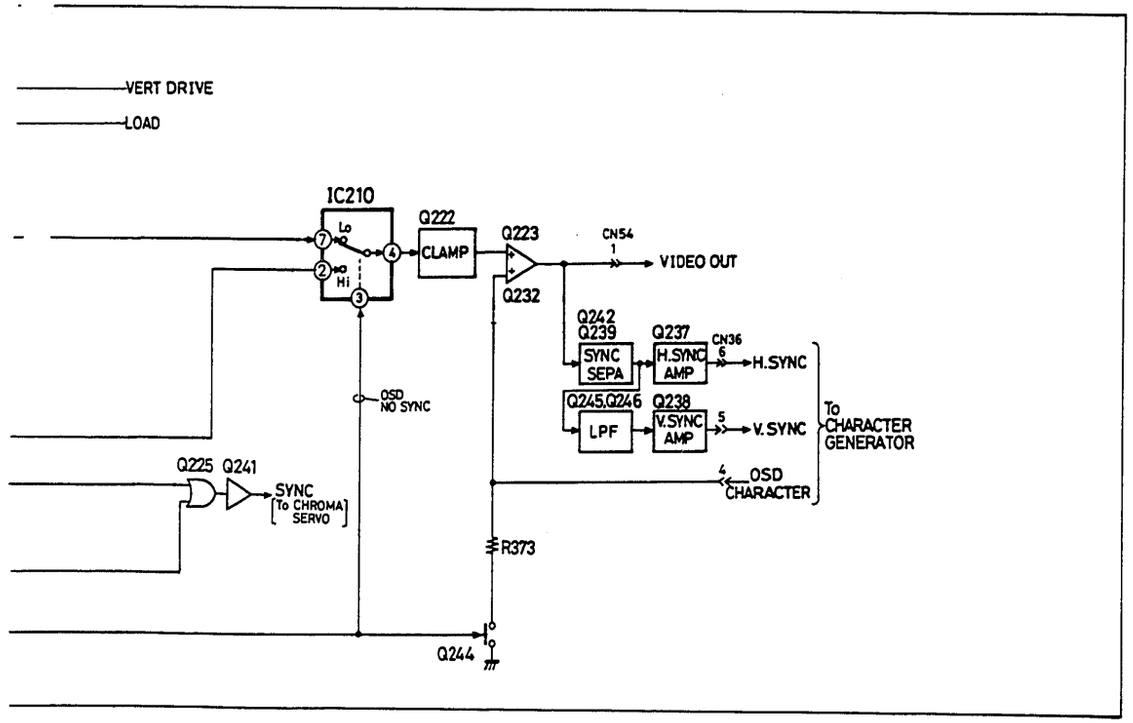
The record monitor output/EE output routes are the same as with conventional VTRs. The signal derived from IC202 pin 25 shown in Fig. 1 flows in the same way in the playback system after passing IC210 pin 7 shown in Fig. 3.

### OSD Operation

The character generator in the system control circuit extracts the H.sync and V.sync from the video final output signal obtained at CN54 pin 1 via Q237 and Q238, and using it as the calculation start base, converts the data in the timer $\mu$P and tape remaining $\mu$P to the OSD characters. The DC level of the characters applied to the video system gets lower and the characters become gray in the OSD mode (OSD modes obtained by pressing the PROGRAM button on the remote control unit when setting clock and programs for the timer, etc.).

### Q248/Q249 operation

With the pulse obtained at the initial stage of V.sync smoothing of the sync detector (IC211), the V.sync is a slightly extended, and this pulse is applied to the PB APC system of the chroma process using Q248 and Q249 to improve the phase characteristics.
This causes the chroma S/N to be improved.



## CHARACTER GENERATOR (IC52)

Fig. 4 shows the character generator (IC52) peripheral circuits.
The character generator receives the data obtained from the timer μP and the tape remaining μP via pins 14 ~ 21 and outputs it at pin 5 as a character signal. The length and width (of the indication position) are determined using the sync signals at pins 7 and 8 as a time base.
Characters obtained in this way are displayed within the range shown in the following table.

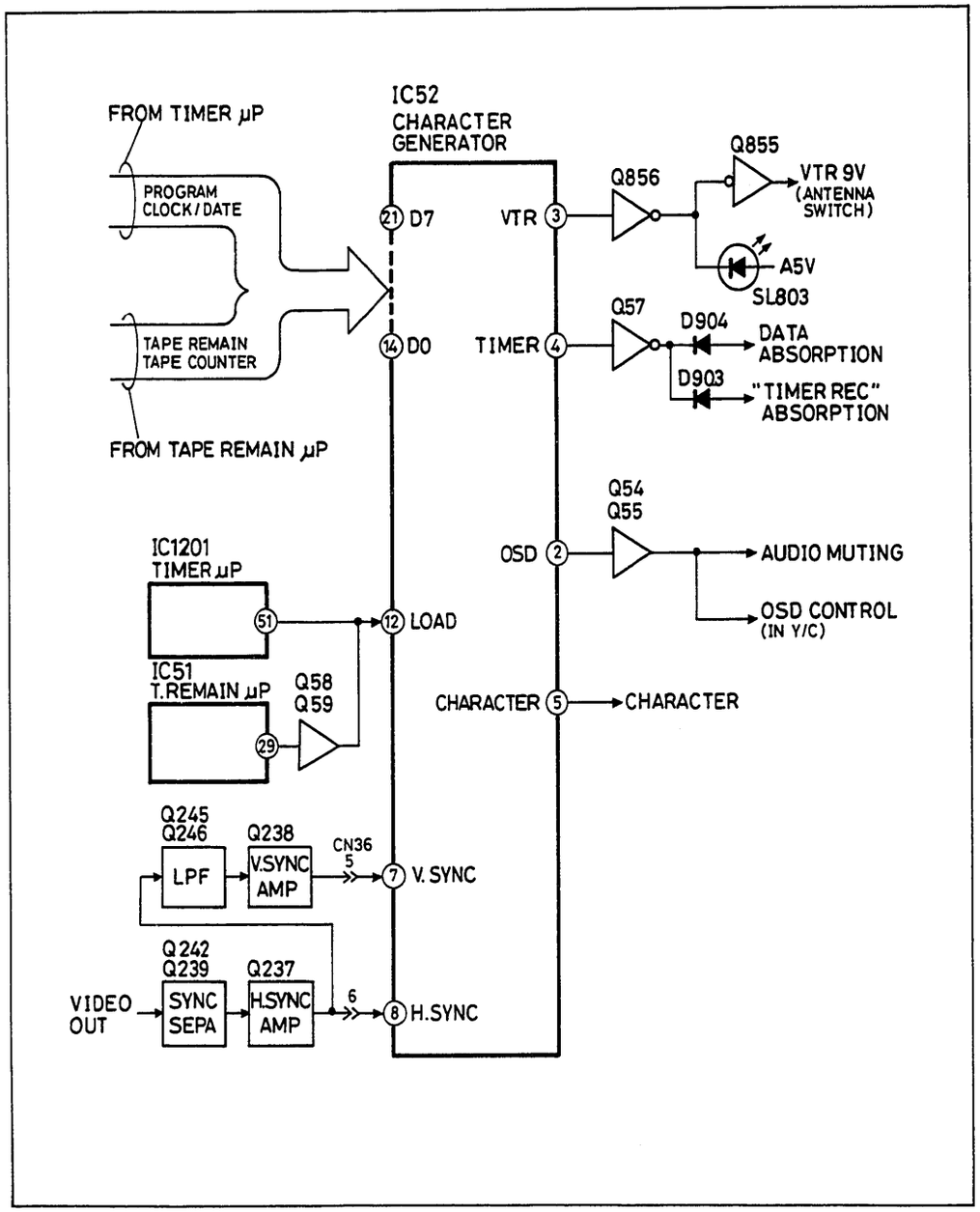



Fig. 4 Character Generator



Fig. 5 shows the relationship between the screen and the display area.

| Indication | 20 characters/1 line x 9 lines |
|---|---|
| Character | 5 (horizontal) x 7 (vertical) dot matrix/ [1.67 μsec] [2.34 μsec] character |
| Character pitch | Horizontally 1 dot, vertically 2 dots |

The address code is composed of 8 bits, D7 (pin 21) is MSB and D0 (pin 14) is LSB, and numbers corresponding to an address are allocated to the code. As a result, when generating a character in address 5, the address code is [00000101].

Address codes are [00000000] (0) to [1011011] (179), and the remaining codes are allocated for processing the character position, size and the character background in the character display area.

Lower 7 bits of D7 ~ D0 are used for the character code.

| D6 (pin 37) | | | Flashing data 1: Flashing |
|---|---|---|---|
| D5 (pin 36) | – | D0 (Pin 31) | Character code |

Character codes are allocated as follows.

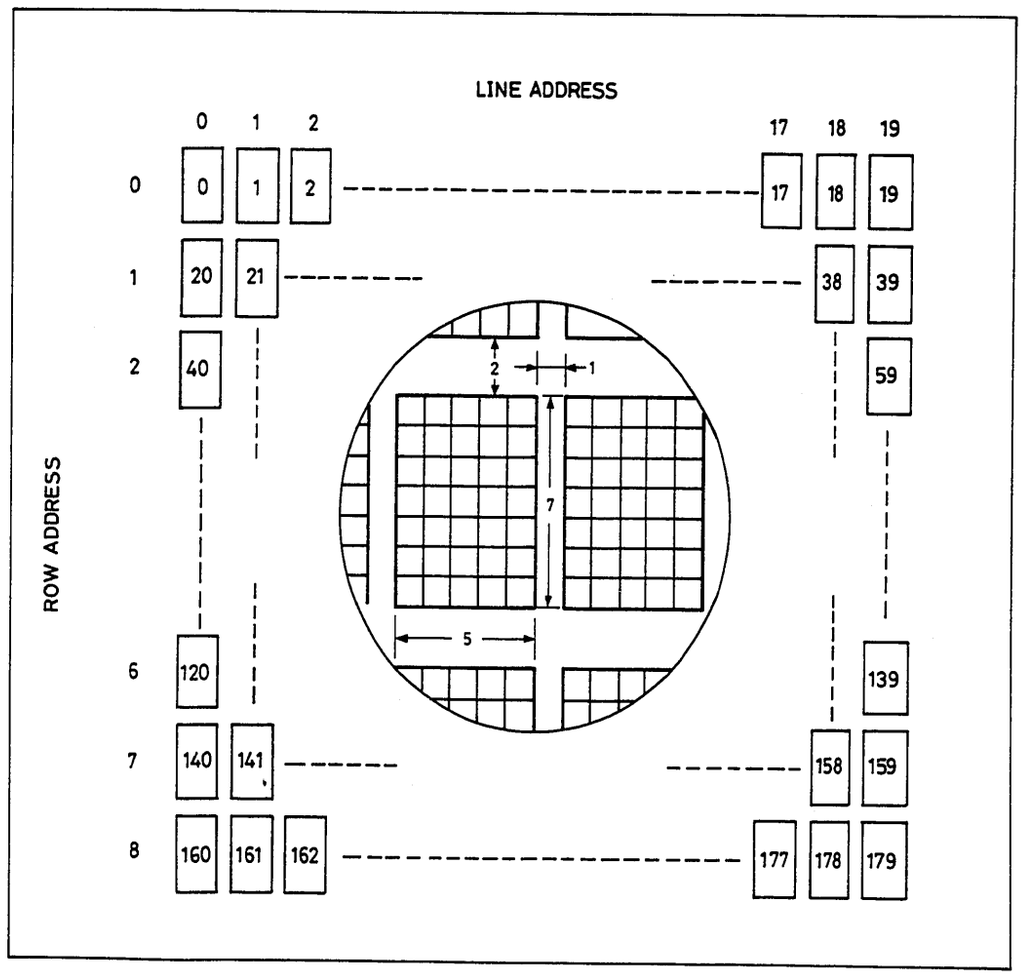
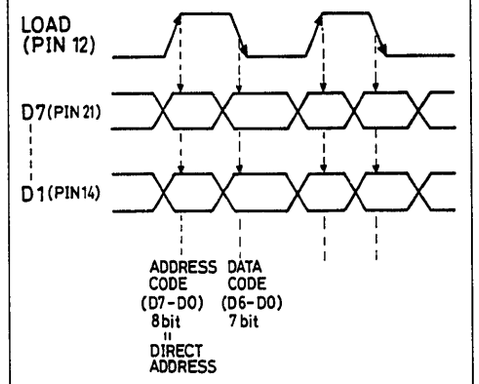



Fig. 5 Relationship Between Screen and Display

**Table 1 Character Codes**

| | D5, D4 / D3-D0 PIN NO. (17) (16) (15) (14) | D5 (PIN 19) 00 | 01 | D4 (PIN 18) 10 | 11 |
|---|---|---|---|---|---|
| 0 | 0 0 0 0 | A | N | 0 | ↑ |
| 1 | 0 0 0 1 | B | O | 1 | ↓ |
| 2 | 0 0 1 0 | C | P | 2 | ← |
| 3 | 0 0 1 1 | D | Q | 3 | → |
| 4 | 0 1 0 0 | E | R | 4 | + |
| 5 | 0 1 0 1 | F | S | 5 | – |
| 6 | 0 1 1 0 | G | T | 6 | * |
| 7 | 0 1 1 1 | H | U | 7 | / |
| 8 | 1 0 0 0 | I | V | 8 | = |
| 9 | 1 0 0 1 | J | W | 9 | & |
| 10 | 1 0 1 0 | K | X | ? | – |
| 11 | 1 0 1 1 | L | Y | ! | – |
| 12 | 1 1 0 0 | M | Z | ' APOS-TROPHE | – |
| 13 | 1 1 0 1 | DOT | : | . PERIOD | – |
| 14 | 1 1 1 0 | ␣ | ■ | □ BACK SCREEN | – |
| 15 | 1 1 1 1 | (BLANK) | [ | ] | – |

**Adress/Data Code Read Timing**




**Dot Interpolation Function**

Fig. 6 shows the dot interpolation.
Characters are difficult to see at positions where the dot patterns are not adjacent at the left and right but are only adjacent diagonally. So, 1 dot is automatically added by interpolation to display characters so that they are easier to see.

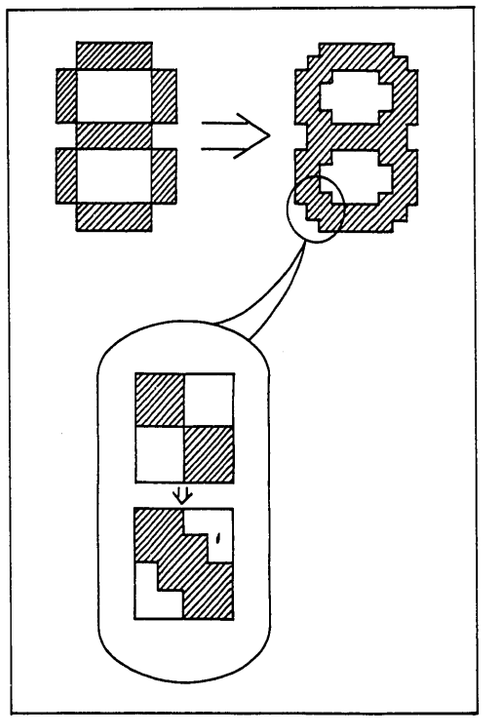
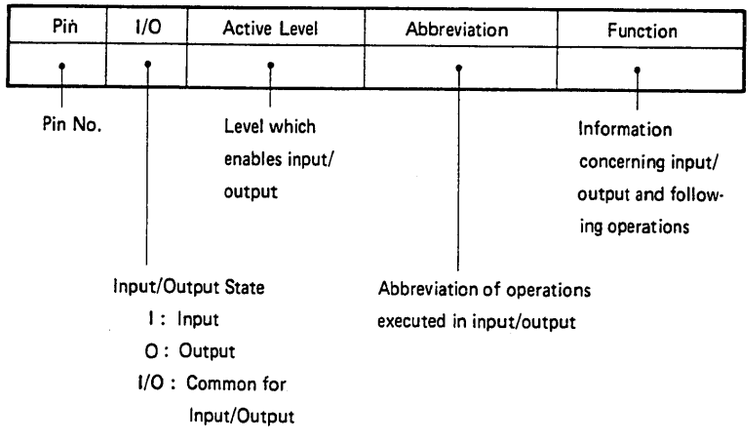


**Fig. 6 Dot Interpolation**



## IC PIN SPECIFICATIONS

| | | | |
|---|---|---|---|
| ICs described: | MB88421-147L | IC851 | (SYSTEM CONTROL μP-A) |
| | MB8847-1257K | IC801 | (SYSTEM CONTROL μP-B) |
| | HD44801-B85 | IC51 | (TAPE REMAIN μP) |
| | MB88303 | IC52 | (CHARACTER GENERATOR) |
| | μPD7519-109 | IC1201 | (TIMER μP) |
| | HD38750-B05 | IC1202 | (REC LEVEL DISPLAY μP) |
| | MB50161-052SP | IC1703 | (TUNING μP) |
| | HA11758 | IC601 | (SLOW CONTROL) |
| | HA11816 | IC602 | (SEARCH CONTROL) |
| | HA11747BNT | IC603 | (CAPSTAN/CYLINDER PHASE CONTROL) |
| | HA11753NT | IC604 | (CAPSTAN/CYLINDER SPEED CONTROL) |



## SYSTEM CONTROL IC (IC851: μP-A) PIN SPECIFICATIONS

Type: MB88421-147L
Functions: Control of circuits and motors in each mode, and detection of mechanism state and trouble.

(Hi : 5V, Lo : 0V)

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1 | I | Lo | $\overline{\text{DEW}}$ | Detects condensation.<br>• Unloads and stops with Lo input<br>• Flashes STOP indicator during Lo period<br>• Inhibits acceptance of all operations during Lo period |
| 2 | I | Hi | FWD END | Detects forward tape end using supply end sensor.<br>Unloads and stops with Hi input |
| 3 | I | Hi | REW END | Detects reverse tape end using take-up end sensor.<br>• Unloads and stops with Hi input |
| 4 | I | ↑ ↓ | REEL LOCK | Detects reel disk rotation.<br>Measures the period of the pulse generated by the Hall elements at the bottom of the reel disk.<br>• Unloads and stops when the period input is more than specified. |
| 5 | I | Hi | CYL LOCK | Detects abnormal cylinder rotation.<br>• Unloads and stops with Hi input |
| 6 | I | Hi | SP | Tape speed data inputs<br>• To light the tape speed indicators.<br>• To switch the current UP signal output time.<br>• To switch the index signal recording time. |
| 7 | I | Hi | LP | |
| 8 | I | Hi | EP | |
| 9 | I | Hi | SAFETY TAB | Detects record enable (safety tab)<br>• Recording operation enable with Hi input (tab provided) |
| 10 | I | Lo | M. STATE 0 | Mechanism state inputs.<br>Become data to control the loading motor and reel motor.<br>*-1: Play, Record, Forward search, Still, Frame advance, Slow, Double Speed Play |
| 11 | I | Lo | M. STATE 1 | |
| 12 | I | Lo | M. STATE 2 | |

| Mode | Detection regulation (1/2 period) |
|---|---|
| Normal Recording/ Play, Search, Double Speed Play | 3 sec or more |
| Still, Slow | ∞ |
| Fast forward, Rewind | 1.5 sec or more |

| | STOP | F. F/REW | REC PAUSE | PB*-1 | REV SEARCH | IN TRANSITION |
|---|---|---|---|---|---|---|
| 10 | Lo | Lo | Hi | Hi | Hi | Hi |
| 11 | Hi | Lo | Lo | Lo | Hi | Hi |
| 12 | Hi | Hi | Hi | Lo | Lo | Hi |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 13 | I | Lo | $\overline{\text{C. PAUSE}}$ | Detects camera pause command.<br>• When this pin is set to Lo during recording, the unit enters the pause mode and it is not possible to release the pause mode using the pause button on the VTR. |
| 14 | I | Hi | INDEX | When the fast forward or rewind operation is performed in the index mode, the mechanism is controlled so that the unit enters the automatic scan operation every time the INDEX signal is detected.<br>Automatic Scan: Visual Search is done for 10 seconds when the INDEX signal is detected and then the unit returns to fast forward or rewind. |
| 15 | I | Hi | C. STATE 0 | Cassette holder state detection inputs.<br>Become data to control the cassette loading motor. |
| 16 | I | Hi | C. STATE 1 | |
| 17 | I | Hi | TIME ON | Detects timer recording command.<br>• When this pin is set to Hi with the timer switch turned on (timer standby), the unit enters the record mode. |
| 18 | I | Lo | $\overline{\text{TIMER STAND-BY}}$ | Detects timer switch state.<br>• When this pin is set to Lo, the timer recording standby mode is judged, and acceptance of other operation mode key inputs is inhibited. |
| 19 | I | Lo | $\overline{\text{MEMORY}}$ | Detects memory stop data for tape counter.<br>• Release the rewind operation to stop the tape running at the programmed position. |
| 20 | I | ↑ ↓ | DATA (B-A) | Communication data buses with μP-B.<br>Data is communicated synchronized with the clock pulse at pin 22.<br>(Refer to Tables 1, 2 on page 46.) |
| 21 | O | ↑ ↓ | DATA (A-B) | |
| 22 | O | ↑ ↓ | CLOCK | Clock pulse to time data communications with pins 20 and 21. |

| | CASSETTE UP | CASETTE IN | IN TRANSITION | CASSETTE DOWN |
|---|---|---|---|---|
| 15 | Lo | Lo | Hi | Lo |
| 16 | Lo | Hi | Lo | Hi |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 23 | O | Lo | CURRENT UP | Signal to be output during phase-matching to erase rainbow caused by video dubbing and to increase the record signal.<br>Outputs in the following operation:<br>STOP PAUSE, STILL, DUB PAUSE → REC PAUSE → REC<br>Output time: 5 sec in SP<br>10 sec in LP<br>15 sec in EP |
| 24 | O | Lo | LINE MUTE | Becomes Lo for approx. 200 msec when changing over the mode to mute the audio line output system. To eliminate pop noise during mode selection. |
| 25 | | | EX | Set μP reference oscillation frequency (3.58 MHz). |
| 26 | | | X | |
| 27 | I | Lo | $\overline{\text{RESET}}$ | Resets μP RAM.<br>• Stop initialized with Lo input. |
| 28 | I | Hi/Lo | INDEX TIME | Sets the search play time during program indexing and sets the F.Fwd or Rewind button (SEARCH) processing.<br>Hi: • Search play time: 30 seconds<br>• Forward or reverse search is done while the F.Fwd or Rewind button is pressed.<br>Lo: • Search play time: 10 seconds<br>• Press the F.Fwd or Rewind button once to perform forward or reverse search. |
| 32 | O | Lo | GND | Grounds μP. |
| 33 | O | Lo | POWER CONT | Power switch state discrimination output.<br>• Set to Lo with the power switch ON. |
| 34 | O | Hi | LM(+) | Cassette loading motor/tape loading motor drive outputs. |
| 35 | O | Hi | LM(−) | |
| 36 | O | Hi | TAPE LOAD | Dual loading motor drivers switching output.<br>Hi: Tape loading driver operates<br>Lo: Cassette loading driver operates |
| 37 | O | Lo | $\overline{\text{2X}}$ | Double speed play control output. |
| 38 – 41 | | | | Reel motor control outputs. |
| 38 | O | Hi | SLACK REMOVAL | Reel motor slack removal control output.<br>• Set to Hi during unloading |

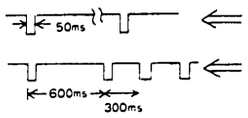
| | STOP | LOAD | UNLOAD | BRAKE |
|---|---|---|---|---|
| Pin 34 | Lo | Hi | Lo | Hi |
| Pin 35 | Lo | Lo | Hi | Hi |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 39 | O | Lo | $\overline{\text{TAKE-UP}}$ | Reel motor take-up control output.<br>• During start : Lo<br>• During stop : Hi |
| 40 | O | Hi | F. FWD/REW | Reel motor high speed rotation control output.<br>• During fast forward, rewind: Hi |
| 41 | O | Hi | REVERSE | Reel motor rotation direction control output.<br>• Forward rotation : Lo<br>• Reverse rotation : Hi |

| Pin \ Mode | STOP | F. FWD | REW | PLAY, RECORD, FWD SEARCH, DOUBLE SPEED | REV SEARCH, REV PLAY | SLACK REMOVAL (UNLOADING) |
|---|---|---|---|---|---|---|
| 38 | Lo | Lo | Lo | Lo | Lo | Hi |
| 39 | Hi | Lo | Lo | Lo | Lo | Lo |
| 40 | Lo | Hi | Hi | Lo | Lo | Lo |
| 41 | Lo | Lo | Hi | Lo | Hi | Hi |

| 42–44 | | | | Tape remaining time calculation control pins |
|---|---|---|---|---|
| 42 | O | Hi | CALC STOP | Tape remaining count control output.<br>• Loading, Stop, Pause : Hi |
| 43 | O | Hi | CALC | Tape remaining count control output.<br>• Recording/Play : Hi |
| 44 | O | Hi | COUNT REVERSE | Tape counter, tape remaining count subtraction control output.<br>• During tape forward running : Lo<br>• During tape reverse running : Hi |
| 45 | O | Lo | $\overline{\text{CYL ON}}$ | Cylinder/capstan start control output.<br>• During start : Lo |
| 46 | O | Hi | $\overline{\text{V. DUB}}$ | Video dubbing mode control output. |
| 47 | O | Lo | $\overline{\text{RECORD}}$ | Record mode control output, REC9V generation |
| 48 | O | Lo | $\overline{\text{A. DUB}}$ | Audio dub mode control output |
| 49 | O | Lo | $\overline{\text{PLAY}}$ | Play mode control output. PB9V generation<br>• Play: Lo |
| 50 | O | Hi | OSC STOP | Bias oscillation control output<br>• Play : Hi<br>• Record pause, Loading : Hi |
| 51 | O | Lo | $\overline{\text{MUTE}}$ | Audio muting control output<br>• Loading, Trick play video dub: Lo |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 52 | O | Lo | $\overline{\text{REVERSE}}$ | Capstan reverse control output<br>• Reverse search, Reverse play<br>Simple phase matching : Lo |
| 53 | O | Lo | $\overline{\text{MONITOR CUT}}$ | Monitor cut control output in loading. |
| 54 | O | ↓ | $\overline{\text{SLOW SPEED UP}}$ | Remote slow speed up pulse output |
| 55 | O | ↓ | $\overline{\text{SLOW SPEED DOWN}}$ | Remote slow speed down pulse output |
| | | | |  <br>• Outputs negative pulses with 50 msec width every time the key is pressed.<br>• Outputs the 2nd pulse 600 msec after key is held down and then outputs negative pulses with 300 msec period. |
| 56 | O | Hi | INDEX REC | When the unit enters the recording, timer recording and IRT recording modes with the INDEX switch turned on, this pin becomes Hi for 1.5 seconds in SP, 2 seconds in LP and 3 seconds in EP after loading is completed, to control recording of the Index signal.<br>(This excludes the time when the record pause is released.) |
| 57 | O | Lo | $\overline{\text{TRICK}}$ | Trick play mode control output |
| 58 | O | Lo | $\overline{\text{SEARCH}}$ | Visual search mode control output |
| 59 | O | Lo | $\overline{\text{F. ADV}}$ | Frame advance mode control output |
| 60 | O | Lo | $\overline{\text{PAUSE}}$ | Pause mode control output |
| 61 | O | Lo | $\overline{\text{SLOW}}$ | Slow mode control output<br>• Slow, Frame advance, Still : Hi |
| 62 | – | Lo | GND | $\mu$P ground |
| 64 | I | Hi | +B | $\mu$P power input (5V) |



## SYSTEM CONTROL IC (IC801: $\mu$P-B) PIN SPECIFICATIONS

Type: MB8847-1257K
Functions: Key input discrimination, Mode indication, Communications with Timer $\mu$P
(Note: L and K are abbreviations of Light and Key.)

[ Hi: 5V, Lo: 0V ]

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1–6 | | | Mode key inputs | |
| 1 | I | ↓ | $\overline{\text{K. F. FWD}}$ | For fast forward mode, forward search mode keys (when the basic mode is play) |
| 2 | I | ↓ | $\overline{\text{K. STOP}}$ | For stop mode key |
| 3 | I | ↓ | $\overline{\text{K. PAUSE}}$ | For pause mode key |
| 4 | I | ↓ | $\overline{\text{K. A. DUB}}$ | For audio dub mode key (not used.) |
| 5 | I | ↓ | $\overline{\text{K. V. DUB}}$ | For insert mode key (not used.) |
| 6 | I | ↓ | $\overline{\text{K. INDEX}}$ | For index search mode key (not used.) |
| 7, 8 | | | Communication lines with system control $\mu$P-A. | |
| 7 | I | ↑ ↓ | DATA (A–B) | Receives data from $\mu$P-A synchronized with lock pulse at pin 4 (Refer to Table 1 on page 46.) |
| 8 | O | ↑ ↓ | DATA (B–A) | Transmits data to $\mu$P-A synchronized with clock pulse at pin 4 (Refer to Table 2 on page 46.) |
| 9–12 | | | Indicator lighting outputs | |
| 9 | O | Lo | $\overline{\text{L. TAPE IN}}$ | Lights "TAPE-IN" indicator |
| 10 | O | Lo | $\overline{\text{L. SP}}$ | Lights "SP" indicator |
| 12 | O | Lo | $\overline{\text{L. LP}}$ | Lights "LP" indicator |
| 13–16 | | | Operation key inputs | |
| 13 | O | ↓ | $\overline{\text{K. EJECT}}$ | Eject key input |
| 14 | O | ↓ | $\overline{\text{K. REC}}$ | Record mode key input |
| 15 | O | ↓ | $\overline{\text{K. REW}}$ | Rewind mode, reverse search mode keys input (when the basic mode is play) |
| 16 | O | ↓ | $\overline{\text{K. PLAY}}$ | Play mode key input |
| 17 | I | Hi | +B | $\mu$P power supply pin |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 20 | — | — | EX TAL | Set μP reference oscillation frequency (3.58 MHz). |
| 21 | — | — | X TAL | |
| 22 | I | Lo | $\overline{\text{RESET}}$ | Resets μP RAM.<br>• Stop initialized with Lo input. |
| 23 | I | ↑ ↓ | CLOCK | Sync pulse to transfer the communication data (pins 33, 34) with μP-A |
| 24 | — | — | — | — |
| 25 | I | Lo | $\overline{\text{K. POWER}}$ | Power switch (binary) input |
| 26 | — | — | — | — |
| 27 | — | — | — | — |
| 28 | O | Lo | $\overline{\text{L. EP}}$ | EP mode indicator lighting output |
| 29 | O | Lo | $\overline{\text{L. POWER}}$ | Power indicator lighting output |
| 30<br>31 | — | — | — | — |
| 32–40 | | | Mode indicator lighting outputs | |
| 32 | O | Lo | $\overline{\text{L. REW}}$ | Indication for rewind mode<br>• Lights during rewind<br>• Flashes during reverse search |
| 33 | O | Lo | $\overline{\text{L. PLAY}}$ | Indication for play mode<br>• Lights during play, trick play, record, audio dub, video dub |
| 34 | O | Lo | $\overline{\text{L. F. FWD}}$ | Indication for fast forward<br>• Lights during fast forward<br>• Flashes during forward search |
| 35 | O | Lo | $\overline{\text{L. REC}}$ | Indication for record mode |
| 36 | O | Lo | $\overline{\text{L. PAUSE}}$ | Indication for pause mode |
| 37 | O | Lo | $\overline{\text{L. STOP}}$ | Indication for stop mode |
| 38 | O | Lo | $\overline{\text{L. V. DUB}}$ | Indication for insert mode (not used.) |
| 39 | O | Lo | $\overline{\text{L.A. DUB}}$ | Indication for audio dub mode |
| 40 | O | Lo | $\overline{\text{L. INDEX}}$ | Indication for program indexing mode. |
| 41 | O | Lo | GND | Grounds μP |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 44 – 47 | | | Communication lines with Timer μP | |
| 44 | I/O | Lo | $\overline{\text{ACK S/T}}$ | Output: Becomes Lo when pin 46 is Lo (Timer μP stands by for data transmission) and μP-B can receive data. μP-B receives data via pin 45 at the rise of pin 46.<br>Input: The μP-B judges that Timer μP is standing by for data reception when this pin is Lo. μP-B transmits data via pin 45 at the rise of pin 47. |
| 45 | I/O | — | DATA S/T | This pin communicates data with Timer μP. (Refer to Tables 3 and 4 on page 48.)<br>Output: μP-B transmits data synchronized with the rise of pin 47.<br>Input: μP-B receives data synchronized with the rise of pin 46. |
| 46 | I | ↑ ↓ | T. READY | Fall: Timer μP stands by for data transmission.<br>Rise: Timer μP transmits data. |
| 47 | O | ↑ ↓ | S. READY | Fall: System control μP-B stands by for data transmission.<br>Rise: System control μP-B transmits data. |
| 48 | – | – | – | — |

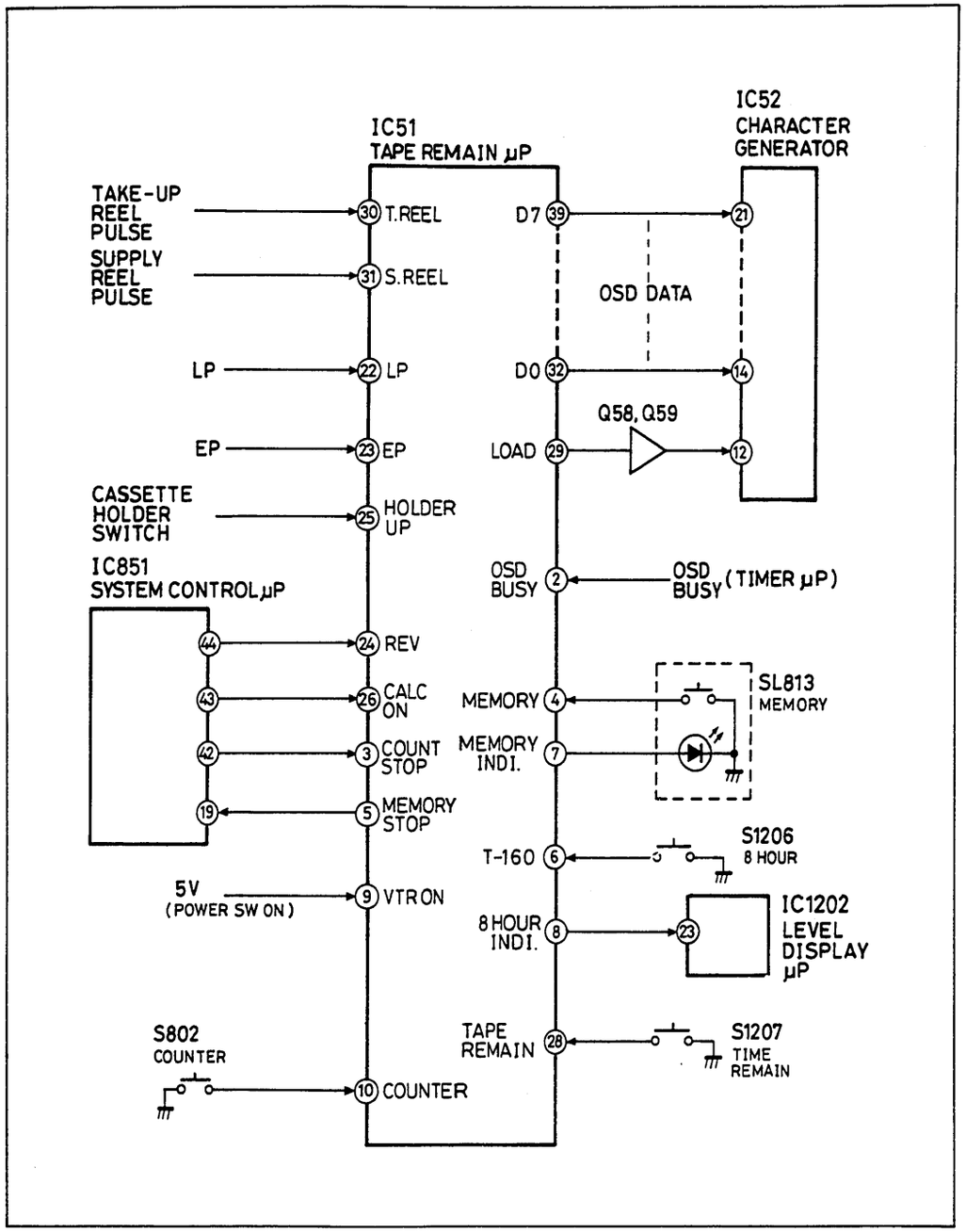
## TAPE REMAINING CALCULATION IC (IC51) PIN SPECIFICATIONS

Type: HD44801B85

Function: Tape remaining calculation and tape counter.

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 40 – 42, 1 | | | Communicating bus with other μPs. | |
| 40 | I/O | – | DATA | Not used |
| 41 | I/O | – | ACK | |
| 42 | I | – | READY | |
| 1 | O | – | READY | |
| 2 | I | Lo | OSD BUSY | Signal showing that Timer μP is outputting OSD data.<br>When this pin is Lo, the tape remaining calculation μP cannot output OSD data. |
| 3 | I | Hi | COUNT STOP | Transition state input pin.<br>Stops the tape remaining calculation in the operation modes (loading, unloading, partial trick play) in which the tape does not travel at the constant speed. The data just before entering the transistion mode is indicated as the tape remaining. |
| 4 | I | Lo | MEMORY | Memory switch input (Binary input)<br>• Input enable when the tape remaining time is not displayed (Memory indicator lights). |
| 5 | I | Lo | T-160 | Input to switch the remaining time calculation. Applies Lo with T-160 tape. |
| 6 | O | Hi | MEMORY STOP | Outputs Hi when the rewind is performed with the memory switch ON and counter changes from "0000" to "9999". The system control μP receives this and sets the unit to the stop mode. |
| 7 | O | Hi | MEMORY INDI | Memory indicator lighting output.<br>Outputs Hi when the input to pin 4 (MEMORY) is effective. |
| 8 | O | Hi | 8 HOUR INDI | Displays "8 HOUR" in the level display when a T-160 tape is loaded. |
| 9 | I | Hi | VTR ON | VTR power switch state input.<br>• When this pin is Lo, the μP output is stopped and the display and data output are not performed. |
| 10 | I | Lo | COUNTER | Counter switch operation input (Binary input)<br>Input to switch to the counter display in the OSD mode. |






**Tape Remain μP Peripheral Circuit**

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 15 | I | Hi | RESET | Reset signal input pin. |
| 16 | O | Lo | Vdd | GND |
| 17 | I | – | OSC1 | Clock frequency set pins. (400 KHz) |
| 18 | I | – | OSC2 | |
| 20 | I | Hi | TEST | Supplies +5V. |
| 21 | I | Hi | Vss | Supplies +5V. |
| 22 | I | Hi | EP | EP tape speed input pin<br>Becomes standard feed speed data during tape remaining calculation. |
| 23 | I | Hi | LP | LP tape speed input pin |
| 24 | I | Hi | REVERSE | Tape reversing signal input pin.<br>Detects the tape travelling direction.<br>Hi: Reverse direction<br>Lo: Forward direction |
| 25 | I | Hi | CASSETTE UP | Cassette holder position input pin.<br>• Stops the tape remaining calculation when the cassette holder is up. The tape remaining time indication by OSD goes off at this time.<br>• The tape remaining time or 4 dashes appear on the TV screen in the tape remaining OSD mode when the cassette holder is down and the VTR is in the stop mode. |
| 26 | I | Hi | CASSETTE UP | Calculation control input pin.<br>Inputs the operation mode in which the tape travels at the constant speed. The tape remaining is calculated only when the tape travels at the constant speed. |
| 27 | I | Lo | COUNTER RESET | Becomes Lo when the reset button is pressed in the tape counter OSD mode and resets the counter to "0000". |
| 28 | I | Lo | TAPE REMAIN | Input to make the tape remaining time be displayed in the OSD mode. |
| 29 | O | ↑↓ | LOAD | OSD indication data transfer timing pulse. It transfers:<br>• Address code at rise, • Displayed character code at fall. |
| 30 | I | Hi | T REEL | Take-up reel rotation input pin (Pin 30).<br>Supply reel rotation input pin (Pin 31).<br>• Receives the reel sensor outputs to detect the take-up reel and supply reel speeds for tape remaining time calculation.<br>• Counts the take-up reel pulse for tape counter. |
| 31 | I | Hi | S REEL | |
| 32–39 | | | | OSD indication data transfer outputs. |
| 32 | O | Hi/Lo | $D_0$ | The outputs compose the address code, counter reading/tape remaining time codes for the OSD indication. (Refer to "CHARACTER GENERATOR IC (IC52) PIN SPECIFICATIONS" for each code.)<br>The address code is transferred at the rise of pin 29 (LOAD) and the numeric code at the fall of pin 29 while pin 2 is Hi. |
| 33 | | | $D_1$ | |
| 34 | | | $D_2$ | |
| 35 | | | $D_3$ | |
| 36 | | | $D_4$ | |
| 37 | | | $D_5$ | |
| 38 | | | $D_6$ | |
| 39 | | | $D_7$ | |



## CHARACTER GENERATOR IC (IC52) PIN SPECIFICATIONS

Type: MB88303

Function: OSD character signal generation

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1 | I | Lo | RESET | IC reset input. |
| 2 | O | Hi | OSD | Becomes Hi in the OSD mode resulting from PROGRAM button operation.<br>• Audio muting<br>• Video OSD control |
| 3 | O | Hi | TV/VTR | Antenna switch selection output.<br>VTR: Hi<br>Outputs Hi when the power switch is turned on, play starts and channels are preset (Select switch ON).<br>• "VTR" indicator lights.<br>• Antenna switch changed to the RF output side. |
| 4 | O | Hi | TIMER | Outputs a Hi pulse (50 msec) at the start of timer recording and at the coupling section of continuous timer recording and causes unloading once to record the Index signal. |
| 5 | O | Hi | CHARACTER | Output with the OSD character data converted to the video waveform. |
| 6 | O | – | BACK-GROUND | Output to control processing of the background for every 1 character area of the OSD. (Not used) |
| 7 | I | Hi | V. SYNC | Signal to be the reference of the vertical position of the OSD characters. |
| 8 | I | Hi | H. SYNC | Signal to be the reference of the horizontal position of the OSD characters. |
| 9 | – | – | EX | Set the LSI reference oscillation frequency. |
| 10 | – | – | X | Character width can be fine adjusted by the constant of this circuit. |
| 12 | I | Hi/LO | LOAD | OSD indication data reception timing pulse<br>• Receives the address data at the rise.<br>• Receives the character data at the fall. |

| Pin | I/O | Active Level | Abbreviation | Function |
|---|---|---|---|---|
| 14 – 21 | | | OSD indication data inputs | |
| 14 | I | | $D_0$ | • Compose the address code and character code. (Refer to Table 1.) |
| 15 | | | $D_1$ | |
| 16 | | | $D_2$ | |
| 17 | | | $D_3$ | |
| 18 | | | $D_4$ | |
| 19 | | | $D_5$ | |
| 20 | | | $D_6$ | |
| 21 | | | $D_7$ | |
| 22 | I | Hi | +B | IC power supply (5V) |

**Table 1 Character Codes**

| | D3-D0 PIN NO. (17) (16) (15) (14) | D5 (PIN 19) 00 | D5 (PIN 19) 01 | D4 (PIN 18) 10 | D4 (PIN 18) 11 |
|---|---|---|---|---|---|
| 0 | 0 0 0 0 | A | N | 0 | ↑ |
| 1 | 0 0 0 1 | B | O | 1 | ↓ |
| 2 | 0 0 1 0 | C | P | 2 | ← |
| 3 | 0 0 1 1 | D | Q | 3 | → |
| 4 | 0 1 0 0 | E | R | 4 | + |
| 5 | 0 1 0 1 | F | S | 5 | – |
| 6 | 0 1 1 0 | G | T | 6 | * |
| 7 | 0 1 1 1 | H | U | 7 | / |
| 8 | 1 0 0 0 | I | V | 8 | = |
| 9 | 1 0 0 1 | J | W | 9 | & |
| 10 | 1 0 1 0 | K | X | ? | – |
| 11 | 1 0 1 1 | L | Y | ! | – |
| 12 | 1 1 0 0 | M | Z | APOS-TROPHE | – |
| 13 | 1 1 0 1 | DOT | : | PERIOD | – |
| 14 | 1 1 1 0 | ␣ | ■ | □ BACK SCREEN | – |
| 15 | 1 1 1 1 | (BLANK) | [ | ] | – |

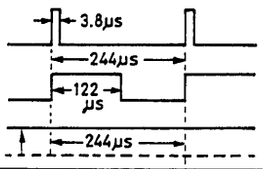


## TIMER CONTROL IC (IC1201) PIN SPECIFICATIONS

Type: μPD 7519-109

Function: Clock/timer, OSD control (channel, present time, programmed time display), 1-year/8-program timer.

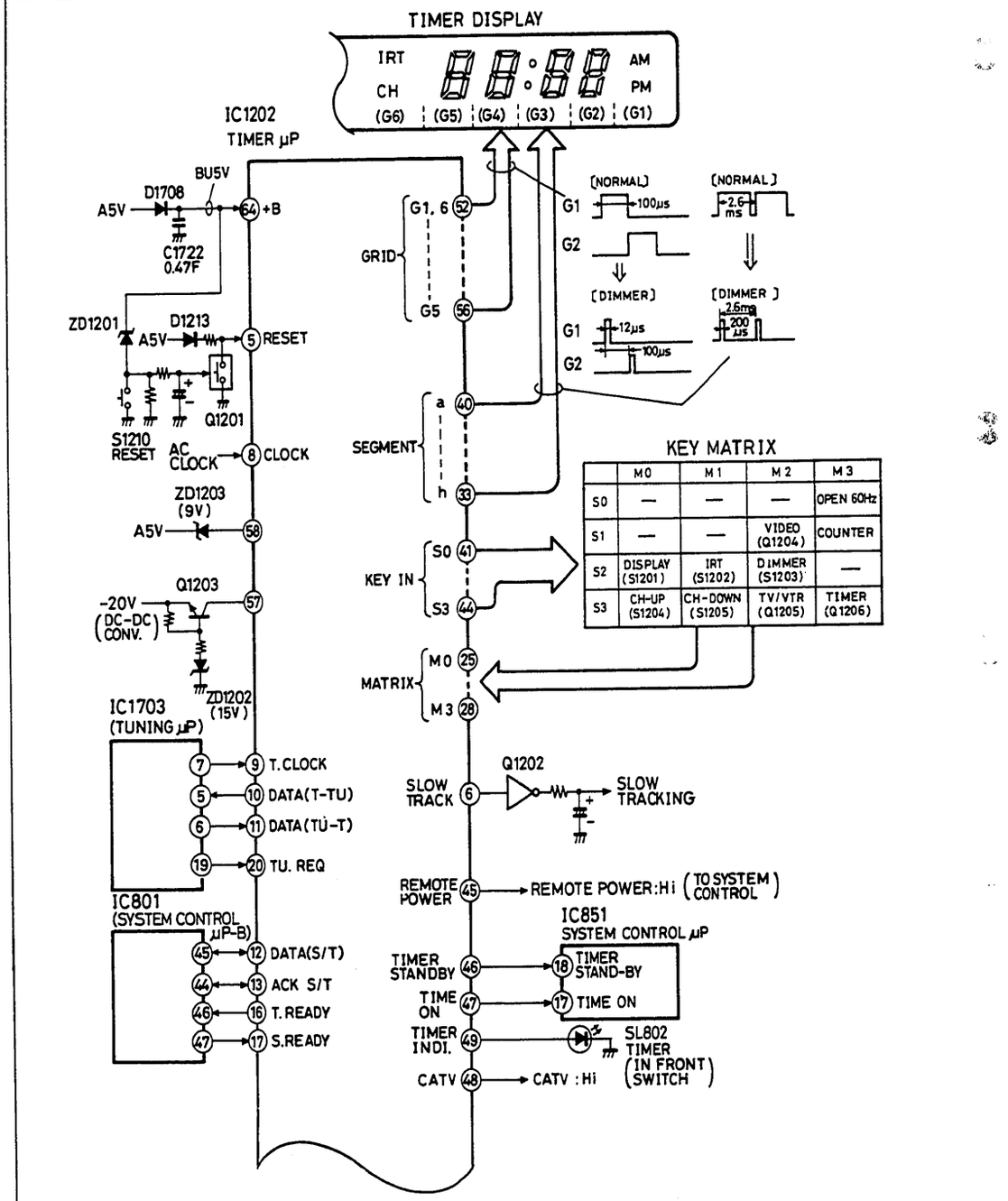
[ Hi: 5V, Lo: 0V ]

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 59 – 62, 1 – 4 | | | OSD indication data transfer output. | |
| 59<br>60<br>61<br>62<br>1<br>2<br>3<br>4 | O | Hi/Lo | $D_0$<br>$D_1$<br>$D_2$<br>$D_3$<br>$D_4$<br>$D_5$<br>$D_6$<br>$D_7$ | Compose the address code and character code required for the OSD indication.<br>(Refer to the character generator (IC52) pin specifications for each code.)<br>While pin 50 is Lo, the address code is transferred at the rise of pin 51 (LOAD), and the character code is transferred at the fall of pin 51 (LOAD). |
| 63 | I | Hi | AC CLOCK | Clock counting AC clock pulse input. |
| 64 | I | Hi | +B | μP power supply pin. Backs μP for 1 hour by use of the backup power supply from the capacitor. |
| 5 | I | Hi | RESET | μP RAM reset input.<br>• Displays "12:00 AM" with reset input. |
| 6 | O | Hi | SLOW TRACK | Tracking control output in the slow play mode. Varies in 64 steps. (1 step: 3.8 s pitck)<br>UP complete ↓↑ Initial ↓↑ DOWN complete<br>  |
| 7 | — | — | — | — |
| 8 | I | — | AC CLOCK | • Clock counting AC clock pulse input.<br>• Power failure detection<br>When the AC clock input interrupts for 24 msec or more, a power failure is detected, and the unit uses the X'tal as the time reference for the clock after 0.5 seconds. |
| 9 – 11, 20 | | | Communicating bus with Tuning μP. | |
| 9 | I | ↑ | T. CLOCK | Timing pulse used for Timer μP to transfer the data (T-TU) to Tuning μP. Tuning μP receives the data at the rise of the pulse. |
| 10 | O | — | DATA (T-TU) | Communication data from Timer μP to Tuning μP. 8-bit serial pulse (Refer to Table 6 on page 50.) |
| 11 | I | — | DATA (TU-T) | Communication data (concerning channel selection, tuning) from Tuning μP to Timer μP.<br>8-bit serial pulse (Refer to Table 5 on page 50.) |
| 20 | I | Lo | TU. REQUEST | Data transfer period signal.<br>Becomes Lo for data communication and data communications are enabled. |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 12, 13, 16, 17 | | | | Communication lines with system control μP. |
| 12 | I/O | — | DATA S/T | Communication data between System Control μP and Timer μP (Refer to Tables 3 and 4 on page 48.) |
| 13 | I/O | Lo | $\overline{\text{ACK S/T}}$ | Output: Becomes Lo when pin 17 is Lo (System Control μP stands by for data transmission) and Timer μP can receive data.<br>Timer μP receives data via pin 12 at the rise of pin 17.<br>Input: Timer μP judges that System Control μP is standing by for data reception when this pin is Lo.<br>Timer μP transmits data via pin 12 at the rise of pin 16. |
| 16 | O | ↑ ↓ | T. READY | Fall: Informs that Timer μP is standing by for data transmission.<br>Rise: Timer μP transmits data via pin 12. |
| 17 | I | ↑ ↓ | S. READY | Fall: Informs that System Control μP is standing by for data transmission.<br>Rise: Timer μP receives the data transmitted from System Control μP via pin 12. |
| 18 | I | Lo | SELECT | Timer μP inputs that it is in the channel preset mode, and performs antenna selection.<br>When switched to "SELECT" with the power turned on, the antenna switch is changed over to the VTR side. |
| 19 | I | Hi | AFT | Displays "AFT" on the OSD screen at Hi when pin 18 is Lo. |
| 14 | — | — | — | — |
| 15 | — | — | — | — |
| 21 | — | — | — | — |
| 22 | I | Lo | WARNING | Safety tab detection input.<br>• Flashes the timer indicator at 1 Hz when a cassette without its safety tab is loaded (or no cassette is loaded) and recording has been programmed. Recording is not possible in this condition. |
| 23 | I | Hi | VTR ON | VTR power supply state detection input.<br>• Operations such as channel selection and record programming, etc. are possible. |
| 24 | — | — | — | — |
| 25<br>26<br>27<br>28 | I | Hi | MAT 0<br>MAT 1<br>MAT 2<br>MAT 3 | Input the scanning pulses at pins 41 ~ 44 via the key matrix and perform the operation according to the key pressed. |
| 29 | I | Lo | EVENT | Grounds via a 1 kohm resistor. |
| 30 | O | — | X'TAL | Set μP reference frequency (4.19 MHz). |
| 31 | I | — | X'TAL | Soft count clock during power failure. |
| 32 | O | Lo | GND | Grounds μP. |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 40 — 33 | | | | Segment control outputs. |
| 40<br>39<br>38<br>37<br>36<br>35<br>34<br>33 | O | Hi | a<br>b<br>c<br>d<br>e<br>f<br>g<br>h | a, IRT<br>b, CH<br>c, AM,<br>d, PM,<br>e,<br>f,<br>g,<br>: — Segments are synchronized with the G1-G5 pulses. |
| 41 — 44 | | | | Key matrix scanning pulses. |
| 41<br>42<br>43<br>44 | O | Hi | S0<br>S1<br>S2<br>S3 | When applied to pin 25 (MAT0) pin 28 (MAT3) via the key matrix, the unit enters the action according to the key operation. (Refer to Table 1 on page 81.) |
| 45 | O | ⊓ | REMOTE POWER | Outputs a 200 msec pulse every time the power key on the remote control unit is operated. |
| 46 | O | Lo | TIMER STAND-BY | Timer recording standby output.<br>• Set to Lo when the timer switch input is accepted when there is a program for the timer. |
| 47 | O | Hi | TIME ON | Timer recording (IRT) command output.<br>Set to Hi during recording while pin 16 is Hi. |
| 48 | O | Hi | CATV | CATV antenna selection output. |
| 49 | O | Hi | TIMER INDI. | Timer indicator lighting output.<br>• Outputs Hi to light the indicator when the timer switch is turned on with "Cassette with safety tab loaded" and "Program set".<br>• Outputs 1 Hz pulse to flash with "Cassette with safety tab broken off loaded" or with "Cassette not loaded". |
| 50 | O | Lo | OSD BUSY | OSD indication data transfer period signal.<br>Becomes Lo for data transfer and stops the data transfer from the tape remaining μP, and the timer μP performs the data transfer. |
| 51 | O | ↑ ↓ | LOAD | OSD indication data transfer timing pulse.<br>• Transfers address code at the rise, and<br>• Character code at the fall. |
| 52 — 56 | | | | 5-phase grid control outputs. |
| 52<br>53<br>54<br>55<br>56 | O | Hi | G1, G6<br>G2<br>G3<br>G4<br>G5 | "AM", "PM": G1 and "IRT", "CH": G6<br>Minute 1's digit.<br>Minute 10's digit.<br>Hour 1's digit.<br>Hour 10's digit. |
| 57 | — | — | — | — |
| 58 | — | — | — | — |




Timer μP Peripheral Circuit

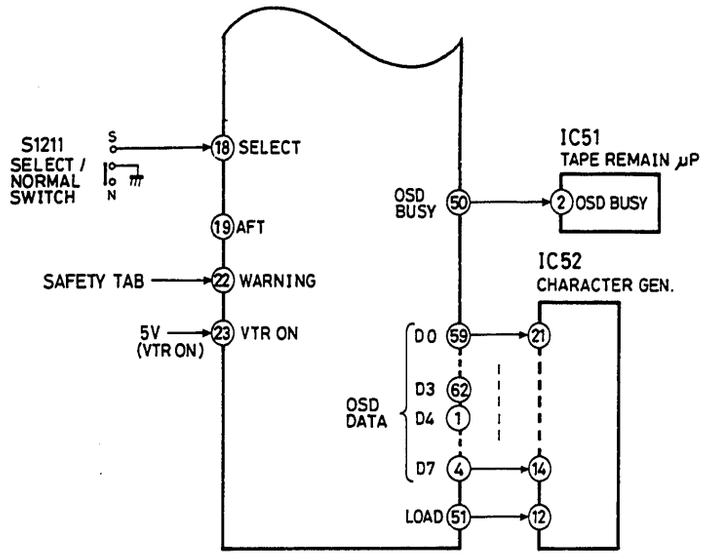


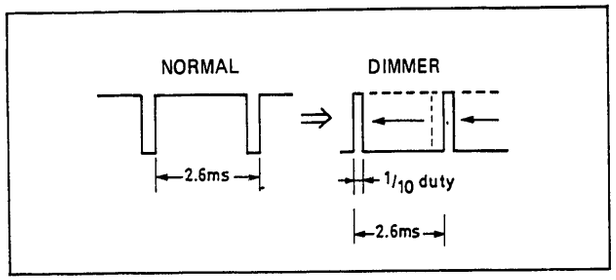

Table 1 Grid/Segment Table

| GRID \ SEGMENT | a (40) | b (39) | c (38) | d (37) | e (36) | f (35) | g (34) | h (33) |
|---|---|---|---|---|---|---|---|---|
| G1 (52) | – | – | AM | PM | – | – | – | – |
| G2 (53) | MINUTE 1's DIGIT | | | | | | | – |
| G3 (54) | MINUTE 10's DIGIT | | | | | | | – |
| G4 (55) | HOUR 1's DIGIT | | | | | | | – |
| G5 (56) | HOUR 10's DIGIT | | | | | | | – |
| G6 (52) | IRT | CH | – | | | | | – |

## REC LEVEL DISPLAY CONTROL IC (IC1202) PIN SPECIFICATIONS HD38750B05

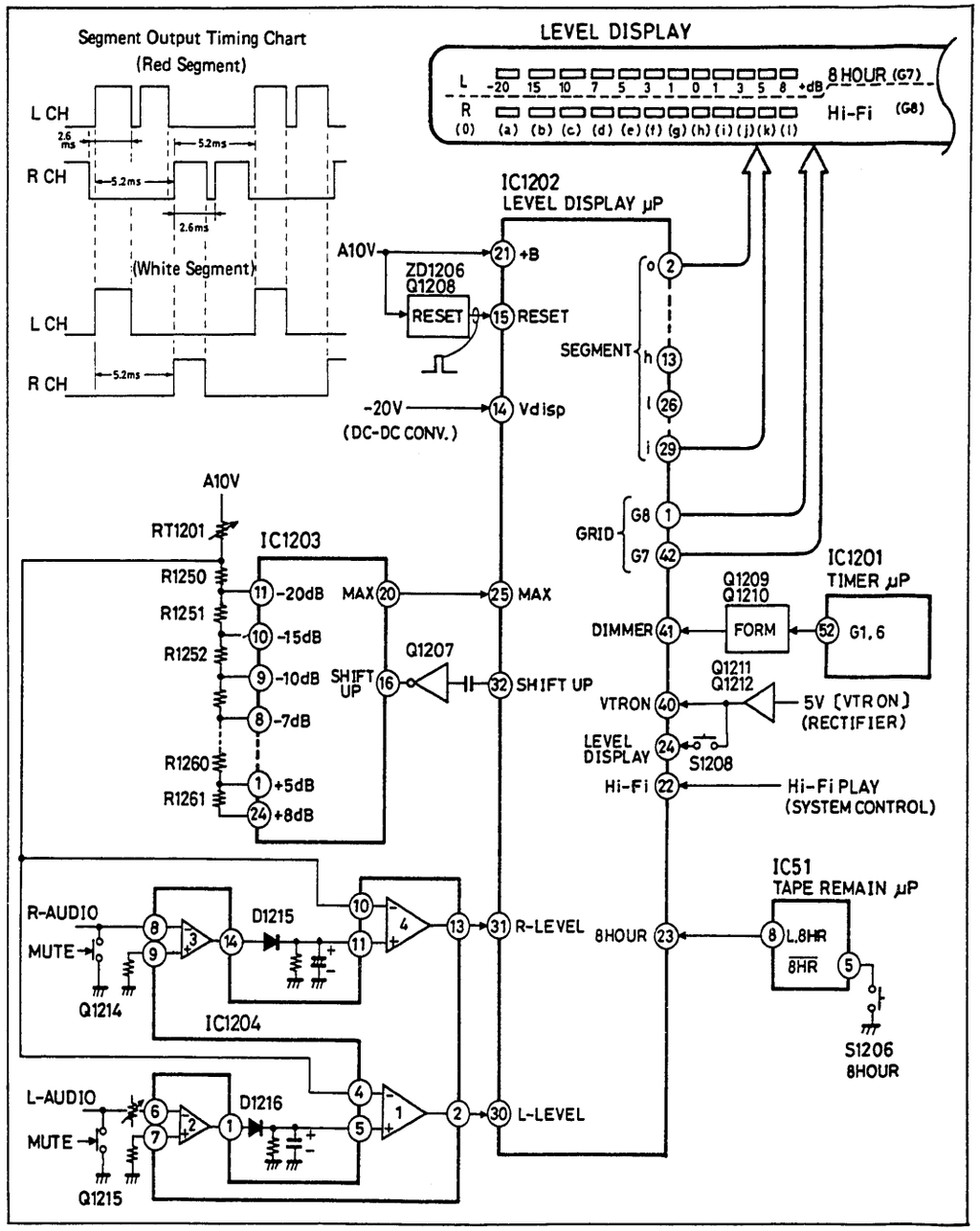
Type: HD38750B05

Function: Audio level decibel (dB) conversion/indication, Hi-Fi/8 HOUR indication

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 42 | O | Hi | G7 | Grid for L, bars in upper row and 8 HOUR area |
| 1 | O | Hi | G8 | Grid for R, bars in lower row and Hi-Fi area |
| 2 – 13, 26 – 29 | | | | Segment drive outputs |
| 2 | O | Hi | o | Light each segment of the level display synchronizing with the grid outputs, G7 and G8.   (Refer to Fig. 1 and Table 1 for locations of segments.) |
| 3 | | | n | |
| 4 | | | p (RED) | |
| 5 | | | m | |
| 6 | | | a | |
| 7 | | | b | |
| 8 | | | c | |
| 9 | | | d | |
| 10 | | | e | |
| 11 | | | f | |
| 12 | | | g | |
| 13 | | | h (RED) | |
| 26 | | | l (RED) | |
| 27 | | | k (RED) | |
| 28 | | | j (RED) | |
| 29 | | | i (RED) | |
| 14 | I | | Vdisp | Negative power supply for diaplay. |
| 15 | I | Hi | RESET | μP RAM reset input. |
| 16 | – | Lo | GND | μP ground |
| 17 | – | Lo | GND | μP ground |
| 18 | I | – | OSC | Sets the μP reference oscillation frequency. |
| 19 | — | — | — | — |

| Segment / Grid | a — g (6) (12) | i , h — 1 (29), (13)(26) | m (5) | n (3) | o (2) | p (4) |
|---|---|---|---|---|---|---|
| G7 (42) | Bars from –20 (a) to –1 (g) of L-CH | Bars from 0 (h) to 8 (1) of L-CH | White numeric section of dB (–20 –1) | 8 HOUR | L | Red numeric section of dB (0 8+) |
| G8 (41) | Bars from –20 (a) to –1 (g) of R-CH | Bars from 0 (h) to 8 (1) of R-CH | — | Hi-Fi | R | — |






**Level Display μP Peripheral Circuits**

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 20 | I | Hi | TESET | Supplies A10V |
| 21 | I | Hi | +B | μP power supply (10V) |
| 22 | I | Hi | Hi-Fi | Input to light "Hi-Fi" in the display when playing Hi-Fi audio. |
| 23 | I | Hi | 8 HOUR | Input to light "8 HOUR" in the display to show that the tape remaining time is normal when T-160 tape is used. |
| 24 | I | Hi | LEVEL DISPLAY | Level display ON/OFF input (binary). |
| 25, 30 – 32 | | | | Audio level dB conversion control pins. |
| 25 | I | Lo | MAX | Level shift completion data from the audio level dB converter (IC1203). |
| 30 | I | ↓ | R-LEVEL | When these pins are Lo, the μP completes the level measurement, stores the shift up pulse at pin 32 and makes the segment pulse output according to the shift up pulse. |
| 31 | I | ↓ | L-LEVEL | |
| 32 | O | Hi | SHIFT-UP | Shift up pulse to perform dB conversion. The dB converter IC1203 shifts up the dB value equivalent to the number of pulses. |
| 40 | I | Hi | VTR ON | VTR power supply state input. The indication output stops with Lo. |
| 41 | I | Hi | DIMMER | Measures the duty of the G1 pulse of the timer μP and judges whether or not the dimmer command has been given to the timer μP. In normal mode: 100 μsec width In dimmer mode: 12 μsec width |

**Audio Level Decibel (dB) Conversion**

The dB conversion of the audio level is performed by the level display μP (IC1202) and the dB converter (IC1203). The audio signal has previously been converted to a DC by the comparator in IC1204 and its peripheral smoothing circuit, and this is compared with the DC level obtained by the dB converter (IC1203) and external resistors. This comparison data is processed by the μP and the corresponding segment output is obtained.

IC1203 sets all pins 11→1 to Lo in sequence corresponding to the pulses input to pin 16. When IC1203 sets all the pins to Lo in turn to memorize the number of the pulses, it sets pin 20 to Lo. IC1202 compares the audio signal level and the output at the dB converter which is shifted up in sequence using IC1204. When the output at IC1204 changes to Lo from Hi (Pin 31 for R channel, pin 30 for L channel), IC2002 stops the shift-up pulse output and generates the segment output equivalent to the number of pulses output up to that time.

L channel and R channel are converted alternately. IC1202 stores the number of pulses output up to the time. When there are more than 8 pulses (equivalent to 0 dB), IC1202 peak holds the segment corresponding to the number of pulses for 2 seconds.



## TUNING IC (IC1701) PIN SPECIFICATIONS

Type: M50161-052SP
Functions: Channel preset, Band/Channel selection, AFT/Muting control & Remote control

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1–4, 13 | | | Communication bus with EAROM | |
| 1 | O | Hi/Lo | $C_3$ | EAROM operation control output. "WRITE", "READ", "ERASE" of data can be controlled between EAROM and Tuning μP according to the state of these 3 pins. (Refer to Table A.) |
| 2 | | | $C_2$ | |
| 3 | | | $C_1$ | |
| 4 | O | ↑ | CLOCK | Timing pulse for data/command transfer |
| 13 | I/O | — | DATA | Channel data line between Tuning μP and EAROM. The input/output are determined by the commands at pins 1, 2, 3, and the channel data is transferred synchronized with with the clock at pin 4. |
| 5 – 7, 19 | | | Communication bus with Timer μP | |
| 5 | I | — | DATA (T-TU) | Communication line of channel selection data, etc. Communicates data in a single direction with Timer μP. The data in each line is 8-bit serial pulse (Refer to Tables 5 and 6 on page 50.) |
| 6 | O | — | DATA (TU-T) | |
| 7 | O | ↑ | T. CLOCK | Timing pulse to transfer the data μPs receive and transfer data at the rise of the pulse. |
| 19 | O | Lo | TU. REQUEST | Data transfer period signal. Held at Lo during data communications to enable communications. |
| 8 | I | Hi | SYNC | When this pin becomes Hi during search, the channel selection is assumed to be completed and sweep-up of the tuning voltage stops. |
| 9-12 | | | Key scan outputs | |
| 9 | O | Lo | $S_3$ | 4-phase scan pulse outputs. When the outputs are applied to the key matrix inputs (pins 27, 28) via the key matrix circuit, the Tuning μP operates as designated by operation keys. (Refer to Table B.) |
| 10 | O | Lo | $S_2$ | |
| 11 | O | Lo | $S_1$ | |
| 12 | O | Lo | $S_0$ | |
| 14 | O | Lo | DEFEAT | Defeat control output during channel selection. Sent to the IF circuit. |
| 15 | O | Lo | GND | μP GND pin. |
| 16 | O | Hi | AFT | AFT control outputs Hi: AFT ON Set to Lo with the BAND key and TUNING key are pressed when presetting channels. |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 17 | O | Hi | $B_1$ | Band selection outputs. |
| 18 | O | Hi | $B_0$ | |
| 20 | O | | TUNING | Tuning control PWM output. This PWM output is smoothed by the external circuit to obtain the tuning voltage. |
| 21 | I | | REMOTE DATA | Remote control input. Tuning μP demodulates this and transfers the command mode to System Control μP via Timer μP. |
| 22 | I | Hi | VOL | IF-S curve detection pin. Receives the S-curve from the IF circuit and.controls sweep-up of the tuning voltage during presetting. |
| 23 | I | Hi | REF | Sets reference voltage for S-curve detection circuit |
| 24 | I | | OSC | Set μP reference frequency. (4.0 MHz) |
| 25 | O | | OSC | |
| 26 | I | Lo | AUTO CLEAR | Resets μP. Clears the data to 0 when the power plug is connected. |
| 27 | I | Lo | MATRIX 0 | Key matrix inputs. (Refer to Table B.) |
| 28 | I | | MATRIX 1 | |
| 29 | | Lo | | GND |
| 30 | I | Hi | +B | Power supply Input (5V). |

| | VH | VL | CATV | UHF |
|---|---|---|---|---|
| $B_1$ | Lo | Lo | Hi | Hi |
| $B_0$ | Lo | Hi | Lo | Hi |

**Table A EAROM Control Commands**

| C1, C2, C3 (3) (2) (1) | Commands and Details |
|---|---|
| Hi Hi Hi | STAND BY . . . Command for the data register and address register to hold their contents. |
| Hi Lo Hi | ERASE . . . Command to erase the address (channel number) data designated in the memory by the address register. |
| Hi Lo Lo | ADDRESS INPUT . . . Command to transfer the address data to the address register. |
| Lo Hi Hi | READ . . . Command for the data register to read the data out from the designated address. |
| Lo Hi Lo | DATA OUTPUT . . . Command to output the data in the data register. |
| Lo Lo Hi | WRITE . . . Command to write the data register into the address area in the address register. |
| Lo Lo Lo | DATA INPUT . . . Command to transfer the input data to the data register. The address register is held. |

**Table B Key Matrix**

| M \ S | S0 (12) | S1 (11) | S2 (10) | S3 (9) |
|---|---|---|---|---|
| MAT 0 (28) | SEARCH | FINE ▲ | SKIP | SELECT |
| MAT 1 (27) | BAND | FINE ▼ | – | – |



## CTL PULSE RECORDING/PLAYBACK, SLOW CONTROL, CAPSTAN REVERSE ROTATION DETECTION IC (IC601) PIN SPECIFICATIONS

Type: HA11758

Function: Intermittent drive output generation

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1 | O | Lo | GND | GND connection terminal. |
| 2 | I | ⎍ | START TIMING PULSE | Inputs periodical pulse which determines the intermittent drive speed. Hi: 66 msec, Lo: Varied by the slow speed button operation. When the pulse becomes wide, the speed gets slow, and when the pulse becomes narrow, the speed gets fast. |
| 3 | I | ⎍ | PB CTL | Playback CTL pulse input. • To generate brake pulse during intermittent drive. • To pass the playback CTL pulse to transmit it to other circuits. |
| 4 | — | — | SLOW TRACKING | Slow tracking circuit delay setting capacitor connection pin. |
| 5 | O | ⎍ | TRACKING REF | Slow tracking circuit reference voltage input. |
| 6 | O | — | SLOW TRACKING | Slow tracking circuit delay setting resistor connection pin. |
| 7 | I | Hi | REVERSE | Reverse operation input. Switches the delay operation from the forward running play in the reverse search and reverse play modes, etc. |
| 8 | I | Hi | SLOW | Intermittent drive control input. Performs ON/OFF operation of the output system in the slow, still and frame operations. |
| 9 | I | Hi | RECORD | Record mode input. Changes over the REC/PLAY switch to REC. |
| 10 | I/O | ⎍ | MM1 (CYL COMPEN) | MM1 time constant circuit. Sets the position to which a pulse is added to correct the horizontal jitter which occurs during intermittent drive. |
| 11 | O | — | MM1 (CTL N. R) | MM1 time constant circuit. Eliminates the CTL pulse noise during normal play. |
| 12 | O | — | MM1 (–1) | MM1 time constant circuit. Switches the delay of the CTL pulse during reverse play. |
| 13 | O | — | MM1 (+2) | MM1 time constant circuit. Excessive reverse rotation occurs during brake in the intermittent drive mode. This pin determines the pulse width to correct it. |

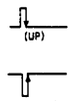
| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 14 | I/O | | MM2 (CYL COMPEN) | MM2 time constant circuit.<br>Determines the pulse width to correct the horizontal jitter which occurs during intermittent drive. |
| 15 | O | — | MM2 (CTL DELAY) | MM2 time constant circuit.<br>Sets the delay of the recording/playback CTL pulse. |
| 16 | I | — | — | — |
| 17 | I | — | MM3 | MM3 time constant circuit.<br>Sets the delay of the recording/playback CTL pulse. |
| 18 | O | | REC CTL | Recording CTL pulse output. |
| 19 | O | Hi | STILL HEAD SWITCH PULSE | Still head switching pulse output.<br>Outputs the pulse in the slow, still and frame advance modes.<br>Outputs a pulse-like signal in the slow and frame advance modes, and Hi in the still mode. |
| 20 | I | | SW30Hz | SW30Hz pulse input.<br>The still head switching pulse is shaped from this pulse. |
| 21 | I | | CTL PULSE | CTL pulse recording input. |
| | O | | | CTL pulse playback output. |
| 22 | O | | CYL. COMPEN | Horizontal jitter correction pulse output during intermittent drive.<br>This is added to the cylinder drive system when the capstan starts. |
| 23 | O | Hi/Lo | ROTATION DIRECTION DET | Capstan rotation direction detection output.<br>Hi: Reverse rotation<br>Lo: Forward rotation |
| 24 | O | | BRAKE | Brake pulse during intermittent drive. |
| 25 | O |  | FEED PULSE | Outputs the pulse in the start/brake periods during intermittent drive to start and control the capstan. |
| 26 | I |  | CFG2 (–) | CFG pulse inputs. |
| 27 | | | CFG2 (+) | |
| 28 | O |  | CFG2 | CFG pulse amplifying/shaping output.<br>SP: 2160 Hz, LP: 1080 Hz,<br>SLP: 720 Hz |
| 29 | I | | CFG1 | This pulse is generated by the CFG installed mechanically advanced in phase by 90° from the CFG2 pulse. |
| 30 | I | 5V | B+ | B+ power supply. |



## SEARCH CONTROL, SLOW CONTROL, $f_H$ CORRECTION AND VERTICAL DRIVE PULSE GENERATION IC (IC602) PIN SPECIFICATIONS

Type: 11816

Function: Noise lock search control CFG/CTL pulse division, slow control, search cylinder output correction ($f_H$ correction) and vert. drive pulse generation.

<table>
<tr><th>Pin</th><th>I/O</th><th>Active Level</th><th>Abbreviaton</th><th>Function</th></tr>
<tr><td colspan="2">1 – 4</td><td colspan="2">Noise lock search CFG/CTL pulse division circuit.</td><td></td></tr>
<tr><td>1</td><td>I</td><td> </td><td>CTL IN</td><td>CTL pulse playback input.</td></tr>
<tr><td>2</td><td>I</td><td> </td><td>CFG IN</td><td>CFG pulse input.</td></tr>
<tr><td>3</td><td>O</td><td> </td><td>CTL OUT</td><td>CTL pulse playback output.</td></tr>
<tr><td>4</td><td>O</td><td> </td><td>CFG OUT</td><td>CFG pulse output.</td></tr>
<tr><td colspan="4"></td><td>Relation between pins 1, 3 and pins 2, 4 is as follows for each mode.<br><table><tr><th>Pin / Mode</th><th>1</th><th>3</th><th>2</th><th>4</th></tr><tr><td>SP REC/PLAY</td><td>30</td><td>30</td><td>2160</td><td>2160</td></tr><tr><td>LP REC/PLAY</td><td>30</td><td>30</td><td>1080</td><td>1080</td></tr><tr><td>EP REC/PLAY</td><td>30</td><td>30</td><td>720</td><td>720</td></tr><tr><td>SP SEARCH</td><td>150</td><td>30</td><td>10800</td><td>2160</td></tr><tr><td>LP SEARCH</td><td>270</td><td>30</td><td>10800</td><td>1200</td></tr><tr><td>EP SEARCH</td><td>450</td><td>30</td><td>10800</td><td>720</td></tr><tr><td>SP x 2 PB</td><td>60</td><td>30</td><td>4320</td><td>2160</td></tr><tr><td>LP x 2 PB</td><td>60</td><td>30</td><td>2160</td><td>1200</td></tr><tr><td>EP x 2 PB</td><td>60</td><td>30</td><td>1440</td><td>740</td></tr></table></td>
</tr>
<tr><td>5</td><td>I</td><td>  </td><td>SLOW SPEED</td><td>Controls the stop period in slow play to select the appropriate slow speed. The UP/DOWN pulse is counted by the internal speed determining U/D counter to vary the speed.</td></tr>
</table>

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 6 | I | Mid/Hi | SEARCH/ DOUBLE SPEED | Search, double speed play control input.<br>Controls the following circuits.<br>• Vert. drive pulse generation<br>• Cylinder $f_H$ correction during search.<br>• Sets the division ratio of the CTL pulse/CFG pulse division circuit. |
| 7 | O | Hi | SLOW | Slow mode control output.<br>Rises at the rise of the CTL pulse and falls at the rise of the SW30Hz pulse when there is input to pin 10. |
| 8 | I | Hi/Mid | EP/LP | Tape speed input.<br>Determines the division ratio of the CTL pulse/CFG pulse division circuit. |
| 9 | I | Hi | F. ADV/ STILL | Frame advance, still mode control input. |
| 10 | I | Hi | SLOW/ STILL | Slow, still mode control input. |
| 11 | I | Hi | REVERSE | Capstan reverse rotation input.<br>Inverts the input to the CTL pulse divider in reverse search. |
| 12 | O | Hi | REEL MOTOR DRIVE | Reel motor drive output in search. |
| 13 | O | Hi | CAPSTAN MOTOR DRIVE | Capstan motor drive output in forward search. |
| 14 | O | ⎍ | SLOW SPEED | Slow mode control pulse output.<br>The frame advance timing and stop period are determined by this pulse to control the slow speed appropriately.<br>Slow speed SP: 1/9, 1/13, 1/17, 1/23, 1/31.<br>LP/EP: 1/5, 1/7, 1/9, 1/13, 1/17, 1/23, 1/31. |
| 15 | I | ▮▮▮▮ | C. SYNC | Composite sync signal input.<br>Search cylinder output correction ($f_H$ correction) circuit input. |
| 16 | O | Lo | GND | GND |
| 17 – 22 | | | $f_H$ correction circuit in search | |
| 17 | I | ⎍ | MM A | Time constant circuit of the monostable multivibrator (MM A) used to extract the horizontal sync signal from the composite sync signal. |
| 18 | I | ⎍ | MM B | Time constant circuit of the $f_H$ correcting trapezoid generation timing control monostable multivibrator (MM B).<br>Generates the trapezoidal wave at the fall. |
| 19 | I | — | TRAPE-ZOID | Sets the rise time of the trapezoidal wave for sample holding.<br>Sampling is performed by this trapezoidal wave and the sampling pulse. |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 20<br>21 | I<br>O | — | NFB | Feedback terminals of the operational amplifier for smoothing/amplifying the sample hold output. |
| 22 | O | DC | $f_H$ COMPE | Output terminal of the cylinder output correction circuit during search. |
| 23 | I | 5V | B+ | B+ power supply connection pin. |
| 24 | I | Hi | SLOW | Enables the output of the $f_H$ correction circuit during still. |
| 25 – 28 | | | Vert. drive pulse generation circuit. | |
| 25 | O | ⎍ | V. DRIVE | Vert. drive pulse generation circuit output. |
| 26 | I | ⎍ | P. WIDTH | Sets the vert. drive pulse width. |
| 27 | I | ⎍ | CH-2 MM | Sets the vert. drive pulse adding position (CH-2). |
| 28 | I | ⎍ | CH-1 MM | Sets the vert. drive pulse adding position (CH-1). |
| 29 | I | 2.5V | INJECTION | Operation power input for the circuit which determines the slow speed and search speed. |
| 30 | I | ⎍<br>Hi | SW30Hz/REC | SW30Hz: Vert. drive pulse generation circuit input.<br>REC Hi: Record mode input. |

## CAPSTAN/CYLINDER PHASE CONTROL IC (IC603) PIN SPECIFICATIONS

Type: HA11747BNT
Function: Capstan phase control, cylinder phase control, assemble operation control.

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1 | — | — | — | — |
| 2 – 6 | | | Capstan phase control circuit. | |
| 2 | O | ⎍⎍⎍ | CAP-PHASE | Capstan phase control PWM wave output. 437 Hz |
| 3 | I | Hi | PWM ADJUST | When Hi is applied to this pin, the duty of capstan phase control PWM wave is set to 50% and the phase control system is disabled.<br>The PWM output is set to 50% in the following operation.<br>• When playing tape with no signal (detected by the circuit built in the IC)<br>• When the cylinder lock is detected (IC604 pin 17: Hi)<br>• Slow mode<br>• Pause mode |
| 4 | I | Lo/$\frac{Vcc}{2}$/Hi | SP/LP/EP | Tape speed data input.<br>The operation values of the built-in counter, divider and the clock pulse, etc. are switched from the tape speed data.<br>SP: Lo, LP: $\frac{Vcc}{2}$, EP: Hi |
| 5 | I | 2.5V | INJECTION | PWM generator power supply. |
| 6 | I | ⎍⎍⎍ | CFG | Capstan phase control CFG input.<br>SP: 720 Hz, LP: 360 Hz, EP: 240 Hz |
| 7 | I | Hi | REC | Recording/playback switching signal input.<br>Record mode: Hi |
| 8 | O | Hi | ASSEMBLE PULSE | Outputs the phase difference between the playback CTL pulse and the vertical sync in the signal to be recorded during assemble operation. A Hi output corresponding to the phase difference is applied to the capstan motor for braking to do phase matching. |
| 9 | I | Hi/Mid | V. DUB ASSEMBLE | 4V: Video dub operation start command input.<br>2V: Assemble operation start command input. |
| 10 | I | — | REF-ADJUST | Fine adjusts the reference signal in phase control.<br>Vcc: +0.43% 1.8V: 0<br>GND: –0.43% |
| 11 | I | Hi | CTL REC INHIBIT | CTL pulse record route shut-off signal.<br>Stops the record CTL pulse output from pin 18 during the loading and record pause modes. |
| 12 – 15 | | | Cylinder tach pulse phase correction and SW30Hz pulse shaping. | |
| 12 | I | ⎍⎍ | CH-1 MM | Time constant of the monostable multivibrator which determines the fall of the SW30Hz pulse for CH-1. |
| 13 | I | ⎍⎍ | CH-2 MM | Time constant of the monostable multivibrator which determines the rise of the SW30Hz pulse for CH-2. |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 14 | I | ⎍⎍ | CYL TACH | Cylinder tach pulse (30 Hz) input.<br>Inputs the signal output from the cylinder motor tach pulse generator to perform cylinder phase control and SW30Hz pulse generation. |
| 15 | O | ⎍⎍ | SW30Hz | Head switching signal SW30Hz pulse output. |
| 16 | I | 5V | B+ | B+ power supply |
| 17 | I | ⎍⎍ | V. SYNC | Vertical sync signal input.<br>• Generates the CTL pulse by dividing the vertical sync signal into 2 and outputs it via pin 18 during recording.<br>• Controls the capstan phase. |
| 18 | O | ⎍⎍ | REC CTL | Record CTL pulse output.<br>The CTL pulse output is inhibited when pin 11 is Hi. |
| 19 | I | ⎍⎍ | TRACKING MM | Time constant circuit of the monostable multivibrator installed in the capstan phase control playback reference signal route. |
| 20 | I | Hi | SEARCH | Visual search mode switching input. |
| 21 | I | ⎍⎍ | PB CTL | Playback CTL pulse input. |
| 22 | I | ⎍⎍ | SEARCH MM | Time constant circuit of the monostable multivibrator circuit which divides the CTL pulse input to pin 21 during search.<br>The period of the CTL pulse in search can be made longer by setting the time constant at pin 22 to more than 33.3 msec. |
| 23 | O | Lo | GND | IC GND terminal. |
| 24 | I | Hi/Lo | PAL/NTSC | Reference clock generating input.<br>Generates the 447 kHz reference clock pulse by dividing the 3.58 MHz signal into 8. |
| 25 | I | ⎍⎍⎍ | REF | Reference clock generating input.<br>Generates the 447 kHz reference clock pulse by dividing the 3.58 MHz signal into 8. |
| 26 | I | 5V | B+ | B+ power supply. |
| 27 | O | ⎍⎍⎍ | CLOCK | 447 kHz clock pulse output.<br>(Produced by dividing the input to pin 25 into 8.) |
| 28 | I | Hi | PWM-ADJUST | Sets the duty of the cylinder phase control output PWM wave to 50% to disable the control.<br>• Search mode<br>• Cylinder lock detection (IC604 pin 17: Hi)<br>• Slow mode |
| 29 | O | ⎍⎍⎍ | CYL-PHASE | Cylinder phase control PWM wave output. 1748 Hz |
| 30 | — | — | — | — |

## CYLINDER/CAPSTAN SPEED CONTROL AND TAPE SPEED AUTOMATIC DETECTION IC (IC604) PIN SPECIFICATIONS

Type: HA11753NT

Function: Cylinder speed control, capstan speed control, tape speed automatic detection, assemble operation CTL pulse counter.

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 1 | I | 5V | B+ | B+ power supply of IC. |
| 2 – 6 | | | Tape speed detection circuit. | |
| 2 | O | Hi | SP | Tape speed detection outputs.<br>• Judge the tape speed from:<br>•The period of the CTL pulse at pin 6 during play, and<br>• The DC level at pin 5 when recording,<br>and outputs the result at pins 2 ~4. |
| 3 | O | Hi | LP | |
| 4 | O | Hi | EP | |
| 5 | I | Lo/$\frac{Vcc}{2}$/Hi | SP/LP/EP | Tape speed selection input pin during recording.<br>Receives the data from the tape speed selector switch via this pin and outputs this data at pins 2 ~ 4 during recording. This input is disabled during play. |
| 6 | I | ⎍⎍⎍ | CTL PULSE | CTL pulse input.<br>The CTL pulse is supplied to the tape speed automatic detection circuit and the assemble operation CTL U/D counter. |
| 7 | I | Hi | $I^2L$ | PWM generator power supply. |
| 8 – 17 | | | Cylinder speed control circuit. | |
| 8 | I | ∿∿∿ | CYL FG | Cylinder FG pulse input. 1.8 kHz.<br>This pulse is used for cylinder speed control and cylinder lock detection. |
| 9 | I | ⎍⎍⎍ | MM 1 | Time constant circuit of the cylinder FG pulse delay monostable multivibrator. Determines the trapezoidal wave circuit charge time. |
| 10 | I | ⎍⎍⎍ | MM 2 | Time constant circuit of the monostable multivibrator (MM 2) which delays the MM 1 output.<br>Sets the discharge time of the trapezoidal wave generation circuit. |
| 11 | I | ⎍⎍⎍ | TRAPEZOID | Time constant circuit used for the circuit which generates the trapezoidal wave for sampling in cylinder speed control.<br>The ramp of the trapezoidal wave can be determined by this time constant. |
| 12 | O | ~~~ | S/H | Circuit to temporarily store the sampling data in the cylinder speed control system. |
| 13 | I | — | $V_{REF}$ | Cylinder servo reference level setting input. |
| 14 | O | — | CYL SERVO | Cylinder servo output.<br>Speed control/phase control addition output. |
| 15 | I | Lo | $\overline{\text{CYL ON}}$ | Cylinder motor start control.<br>The cylinder starts when this pin becomes Lo by the command from the system control and the cylinder stops when it is Hi. |



| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 16 | I | ~~~ | CYL PHASE | Cylinder phase control signal input.<br>This signal is added to the speed control signal in this IC and is output via pin 14. |
| 17 | O | Hi | CYL LOCK | Cylinder abnormal stop data output.<br>When the period of the CYL FG pulse input via pin 8 becomes longer, the cylinder stops and Hi is output. |
| 18 – 24 | | | Assemble, video dub operation control circuit. | |
| 18 | O | Hi | ASSEMBLE | Assemble operation period signal.<br>Outputs Hi when the U/D counter is doing the assemble operation. |
| 19 | O | Hi/Mid | V. DUB ASSEMBLE | Hi: Video dub operation period output.<br>Mid: Assemble operation period output. |
| 20 | I/O | Lo | REC CHECK | Input; Record check operation start trigger.<br>The counter starts counting up.<br>Output: Record check operation period.<br>The counter counts up and down. |
| 21 | O | Lo | GND | IC GND terminal. |
| 22 | I | ⎍ | ASSEMBLE MM | Generates the pulse with a certain width which can be the substitute output to prevent a malfunction due to miscounting of the CTL pulses in the assemble mode. |
| 23 | I | Hi | UP COUNT | CTL counter up count control input during the assemble operation.<br>Becomes Hi by the signal during the reverse operation and the counter counts up the CTL pulses. When this pin becomes Lo, the counter counts down the CTL pulses. |
| 24 | I | Hi | PAUSE | Counter operation control.<br>When the pause signal is applied, the counter operates. |
| 25 | I | Lo/$\frac{Vcc}{2}$/Hi | PB/REC/ V. DUB | Switches the built-in circuit according to the input voltage level.<br>PB: Lo, REC: $\frac{Vcc}{2}$, V. DUB: Hi. |
| 26 – 32 | | | Capstan servo control circuit. | |
| 26 | I | ~~~ | CAPST-PHASE | Capstan phase control signal input.<br>The signal is applied to pin 26 and added to the speed control signal. |
| 27 | I | — | CAPSTAN SPEED | Capstan speed set. |
| 28 | O | ~~~ | CAPST-SERVO | Compound output of the capstan phase/speed control signals which is supplied to the cylinder motor. |
| 29 | O | — | D/A CONV | Converts the output of the capstan phase control D/A converter. |

| Pin | I/O | Active Level | Abbreviaton | Function |
|---|---|---|---|---|
| 30 | O | ⎍⎍⎍_ | 1/3 CFG | CFG division output.<br>Divides the CFG signal input to pin 32 into 3 and outputs it.<br>SP: 720 Hz, LP: 360 Hz, EP: 240 Hz |
| 31 | I | Hi | SLOW | Slow mode control.<br>Switches the clock pulse supplied to the counter in the capstan speed control system.<br>Normally: 447 kHz clock<br>During slow: 447 x 3/4 kHz clock |
| 32 | I | ⎍⎍⎍ | CFG | CFG pulse input.<br>Supplies the CFG pulse to the capstan speed control system.<br>SP: 2160 Hz, LP: 1080 Hz, EP: 720 Hz |
| 33 | I | Lo/Hi | NTSC/PAL | NTSC/PAL switching control input.<br>NTSC: Lo, PAL: Hi |
| 34 | I | $\frac{Vcc}{2}$ | INJECTION | Power supply for PWM wave generator in the capstan speed control system. |
| 35 | I | ⎍⎍⎍ | 1/8 fsc | Clock input for the REF counter in the capstan speed control system. |
| 36 | — | — | — | — |
| 37 | I/O | — | REF ADJUST | Fine adjusts the reference signal in the speed control system.<br>Vcc: 0.43%, 1/2Vcc: 0%, GND: −0.43% |
| 38 – 42 | | | | CTL pulse play amp. |
| 38 | I | ⊥⊤⊥ | CTL PULSE ⊕ IN | CTL pulse play input.<br>The CTL pulse is amplified by the internal play amp and is output via pin 42. |
| 39 | I | — | CTL PULSE ⊖ IN | CTL pulse play amp bias input. |
| 40 | O | Lo | GND | CTL pulse play amp GND. |
| 41 | O | | CTL FB | CTL pulse play amp feedback resistor connecting terminal. |
| 42 | O | ⊥⊤⊥ | CTL PULSE OUT | CTL pulse play amp output.<br>3Vp-p. |



HITACHI

**HITACHI SALES CORPORATION OF AMERICA**
Eastern Regional Office
1290 Wall Street West, Lyndhurst, New Jersey 07071, U.S.A.
Tel. 201-935-8980

**Mid-Western Regional Office**
1400 Morse Ave., Elk Grove Village, III. 60007, U.S.A.
Tel. 312-593-1550

**Southern Regional Office**
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Tel. 404-763-0360

**Western Regional Office**
401 West Artesia Boulevard, Compton, California 90220 U.S.A.
Tel. 213-537-8383

**HITACHI SALES CORPORATION OF HAWAII. INC.**
3219 Koapaka Street. Honolulu, Hawaii 96819, U.S.A.
Tel. 808-836-3621

**HITACHI (HSC) CANADA INC.**
3300 Trans-Canada Highway, Pointe Claire, Quebec,
H9R 1B1, Canada
Tel. 514-697-9150

**Hitachi Sales Centroamericana, S.A.**
San Rafael de Escazu, (Apartado 10272), San Jose,
Costa Rica
Tel. 28-2011, 28-0037

**Hitachi Sales Corporation de Panama, S.A.**
Nuevo Reparto el Carmen, Calle Ramon Arias y Calle B
Edificio Brasil 100, (Apartado 7657) Panama 5
Panama City, Rep. of Panama
Tel. 61-3100, 61-4305

**Hitachi Sales de Chile Cia., Ltda.**
Av. Mexico, 0183, Casilla 9793, Correo Central
Santiago, Chile
Tel. 774165

**HITACHI Ltd. TOKYO JAPAN**
Head Office: THE HITACHI ATAGO BLDG.
No. 15-12, 2-Chome Nishi-Shinbashi
Minato-Ku, Tokyo 105, Japan
Tel. Tokyo (03) 502-2111

**VT-89A TK No.2180E TOKAI**

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